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WYDZIAŁ ELEKTRYCZNY

Ph.D. Thesis

Reliability Improvement of High Performance Power Supplies

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Reliability Improvement of High Performance Power Supplies

Abstract

Power electronic converters are used in the modern world so commonly that they significantly impact people's lifestyles. They are used in electric vehicles, renewable energy sources, base transceiver stations, aircraft and naval board power supply systems, AC and DC microgrids, servers, and many more applications. So common utilization of advanced power electronics makes the reliability improvement of power supplies a pressing matter.

Demand for reliability improvement of power electronic converters is even higher in the case of High Performance Power Supplies, like aircraft/naval board power supply systems, mining equipment, or base transceiver stations. In this dissertation, a different niche of High Performance Power Supplies was focused on - plasma processing systems. Without plasma processing, there would not be any integrated circuits, flat panel displays, solar panels, architectural glass, nor any other landmarks of XXI century. Thus, various plasma processing techniques and systems, as well as power converter topologies for such application, are discussed in this dissertation to bring this topic to a broader audience.

Discussion acts as an introduction for comparative analysis on methods for reliability improvement of High Performance Power Supplies. This led to the conclusion that Design for Reliability (DfR) is the most suitable approach for those devices. Unfortunately, closer evaluation of engineering workflow based on this methodology indicates that DfR procedure is too time-consuming, making it unsuitable for short lifespan projects, typical for the plasma processing industry. Therefore, a modified DfR procedure was proposed, which shifts the pressure from simulation study onto extensive laboratory testing. Moreover, the proposed modification introduces the concept of the *Reliability Maintenance* to the DfR procedure, which ensures that the reliability of all mass-produced power supplies will not be worse than in the first unit. The proposed modified DfR procedure resulting from this Ph.D. thesis is being implemented in TRUMPF Huettinger Sp. z o. o.

Research presented in this dissertation was meant to support implementation of modified DfR procedure. Thus, the reliability model for *SiC* power MOSFET in

$SOT-227B$ housing was identified. For this purpose following methodologies were introduced:

- Accelerated lifetime testing of SiC power MOSFET, which bases on i.a. grouping of similar failure modes, to reduce number of required accelerated lifetime tests.
- Power cycling of SiC power MOSFET, which bases on linear mode operation of tested MOSFET, and utilization of conduction losses to heat up tested structure.

Moreover, a test bench for the accelerated lifetime testing according to given methodologies, was designed and assembled. Test results were used to develop the reliability model, which allows plotting a density function for the probability of failure of SiC power MOSFET in $SOT-227B$ housing, for given operating conditions. Such probability density function can be further used for useful lifetime estimation of SiC power MOSFET, which defines a period of maintenance of High Performance Power Supply.

The dissertation is ended with a case study analysis depicting practical utilization of modified DfR procedure. For this purpose:

- a Power Electronic Building Block (PEBB) was designed,
- a Reliability Oriented Comparative Test (ROCT) of Si MOSFET drivers was conducted.

Keywords: Reliability Engineering, Semiconductor Device Reliability, Silicon Carbide, Power Electronics, Energy Conversion, Energy Transformation, AC/DC Power Converters, DC/DC Power Converters

Zwiększanie niezawodności przekształtników energoelektronicznych specjalnego przeznaczenia

Streszczenie

W nowoczesnym świecie, przekształtniki energoelektroniczne są wykorzystywane tak powszechnie, że mają one trwały wpływ na kształt ludzkiego życia. Stosuje się je w pojazdach elektrycznych, odnawialnych źródłach energii, stacjach bazowych systemów łączności bezprzewodowej, sytemach zasilania pokładowego statków i samolotów, mikrosieciach prądu stałego i zmiennego, serwerowniach i wielu innych aplikacjach. Tak powszechne wykorzystanie przekształtników energoelektronicznych, sprawia że zwiększanie niezwodności przekształników energoelektronicznych staje się coraz bardziej palącym zagadnieniem.

Nacisk na zwiększanie niezawodności jest szczególnie wyraźny w przypadku Przekształtników Energoelektronicznych Specjalnego Przeznaczenia, takich jak właśnie systemy zasilania pokładowego, maszyny górnicze czy stacje bazowe systemów łączności bezprzewodowej. W tej rozprawie, skupiono się na innej nietypowej niszy zastosowań zasilaczy - systemach do obróbki plazmowej. Bez nich nie byłoby układów scalonych, płaskich ekranów, paneli fotowoltaicznych i innych sztandarowych produktów XXI wieku. Aby przybliżyć tę tematykę szerszemu gronu odbiorców, w pracy przedstawiono główne typy procesów i systemów obróbki plazmowej, oraz jakie topologie przekształtników mogą być stosowane w takich systemach.

Ta dyskusja stanowi wstęp do analizy metod zwiększania niezawodności Przekształtników Energoelektronicznych Specjalnego Przeznaczenia. Na jej podstawie wywnioskowano, że metodyka projektowania zorientowanego na niezawodność (*ang. Design for Reliability (DfR)*) jest najbardziej adekwatnym rozwiązaniem tego problemu. Niestety, bliższa ocena procesu projektowego, opartego na tej metodyce, wskazuje, że jest on zbyt czasochłonny, aby sprostać wymogom projektów o krótkim czasie życia. W związku z tym, zaproponowano modyfikację procesu projektowania niezawodnościowego, przenosząc nacisk z badań symulacyjnych na badania laboratoryjne prototypu. Ponadto, zaproponowana modyfikacja wprowadza do procedury DfR pojęcie *utrzymania niezawod-*

ności, które ma zapewnić, że niezawodność kolejnych serii produkowanych urządzeń nie będzie gorsza niż pierwszej sztuki. Zaproponowana procedura jest przedmiotem wdrożenia efektów tej rozprawy doktorskiej w firmie TRUMPF Huettinger Sp. z o. o.

Badania laboratoryjne przedstawione w tej rozprawie, posłużyły do wprowadzenia w życie zmodyfikowanej procedury DfR, poprzez opracowanie modelu niezawodnościowego tranzystora SiC MOSFET w obudowie $SOT-227B$. W tym celu opracowano metodyki:

- Przeprowadzania testu przyspieszonego tranzystora SiC MOSFET, która zakłada m.in. grupowanie podobnych mechanizmów awarii, w celu zmniejszenia liczby wymaganych testów przyspieszonych.
- Przeprowadzania testu cyklowania mocą tranzystora SiC MOSFET, która zakłada wprowadzenie badanego tranzystora w zakres pracy liniowej i wykorzystanie strat przewodzenia do podgrzewania badanego elementu.

Ponadto zaprojektowano i wykonano stanowisko badawcze, na którym przeprowadzono badania laboratoryjne według wymienionych wyżej metodyk. Wyniki badań posłużyły do opracowania modelu niezawodnościowego, który umożliwia wyznaczenie rozkładu gęstości prawdopodobieństwa tranzystora SiC MOSFET w obudowie $SOT-227B$, dla określonych warunków pracy. Na jego podstawie można określić użyteczny czas życia tranzystora, a co za tym idzie - okres po którym należałoby przeprowadzić konserwację przekształtnika specjalnego przeznaczenia.

Rozprawę kończy studium przypadku, obrazujące praktyczne wykorzystanie zmodyfikowanej procedury projektowania niezawodnościowego. Do tego celu opisano

- proces projektowy bloku energoelektronicznego (*ang. Power Electronic Building Block (PEBB)*),
- badania porównawcze niezawodności sterowników bramkowych tranzystorów Si MOSFET.

Słowa kluczowe: Inżynieria Niezwodnościowa, Niezawodność Elementów Półprzewodnikowych, Węglik Krzemu, Energoelektronika, Przetwarzanie Energii, Przekształcanie Energii, Przekształtniki AC/DC, Przekształtniki DC/DC

Contents

Chapter 1

Introduction

Plasma processing techniques are routinely used in the manufacturing of various types of commonly used equipment – from corrective lenses, through drills, surgical equipment and architectural glass, up to integrated circuits. Thus, the modern world would hardly be recognizable without plasma processing techniques. This broad scope of applications is mainly covered by two types of plasma processes: Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD), in both of which the plasma has to be excited and sustained by a dedicated High Performance Power Supplies (HPPSs). The wide variety of manufacturing processes where plasma is used has triggered the development of a large family of plasma power supplies, from devices using straight Direct Current (DC) or Pulsed Direct Current (Pulsed DC) up to the Radio Frequency (RF) and Very High Frequency (VHF) ranges.

Research presented in this thesis focuses on the reliability improvement of HPPSs for plasma processing, and is meant to prove following thesis:

Thesis: It is possible to develop a probabilistic model, describing a probability of failure of Silicon Carbide (SiC) power MOSFET, which enables reliability evaluation of newly developed High Performance Power Supply (HPPS) for plasma processing, according to the modified Design for Reliability (DfR) procedure.

To prove this thesis following goals were defined:

1. Analysis of operating conditions of HPPSs for plasma processing systems, and power converter topologies used for such applications.
2. Proposal of the DfR procedure, suitable for development of new HPPSs.
3. Design and start-up of the Accelerated Lifetime Test (ALT) of SiC MOSFET in $SOT-227B$ housing.
4. Identification of reliability model, based on the ALT results.

This dissertation is organized as follows. In chapter 1 major types of plasma processes and their applications in the modern industry are presented. Discussion acts as a background for description of the major types of power converters used in such applications. Moreover, it shows why high reliability is one of the key requirements for modern HPPSs. Next, in chapter 2, definition of the reliability is introduced and leading strategies for reliability improvement of modern power electronic converters are compared. Analysis presented in chapter 2 indicates that the DfR a most suitable approach for HPPSs. Moreover, the DfR procedure for short lifespan projects - typical for the plasma processing industry - is also presented in this chapter. Discussion ends with substantiation why research focuses on SiC power MOSFETs. The detailed description of reliability modelling of the SiC power MOSFET in $SOT-227B$ housing is given in chapter 3. This chapter starts from preparation of the ALT, and it is being continued with the test results analysis and post-failure examination of SiC MOSFETs subjected to the ALT. Discussion ends with the recognition of proper mathematical distribution, which could be further used as a reliability model for tested SiC MOSFETs. Afterwards, in chapter 4, the case study analysis for chosen aspects of proposed DfR procedure is presented. Conclusions and summary for this thesis are given in chapter 5.

1.1 Plasma processing techniques

The plasma processing technique is used to change the properties of the surface exposed to the plasma. This may involve covering a bare surface of, e.g., a metal with single or multiple thin layers of another material. The modification of a surface with a thin coating, called also *deposition*, is used in the manufacture of many of the industrial products we encounter every day. In the case of metal elements, such as drills, the coating can consist of TiN, CrN, or a mixture thereof [1]. Bio-compatible protective layers for joint implants in medical applications are manufactured in a similar process [2], whereas another example are a thin optical coatings, which nowadays are an inherent part of the glass industry. Windows and glass facades are made of what is known as Low-E glass, where a thin multi-layer coating helps to control the heat transfer between the outside and inside of a building while providing satisfactory transparency for visible light [3]. Similar examples of widely used coatings are Ultraviolet (UV) shields (e.g. for glasses) [4], anti-reflective coatings on glass surfaces (e.g. for architectural glass) [5] or reflective surface manufacturing (e.g. for industrial mirrors) [6]. Plasma-deposited decorative coatings are routinely applied on a variety of products such as bathroom taps, mobile phones and eyeglasses [7–9].

Plasma can also be used for the removal of a defined thickness of a surface or for the precise, selective removal of certain parts of a substrate. By means of non-selective surface removal one can obtain a defect- and contaminant-free surface (called also *dry cleaning* or *plasma cleaning*), to ensure good adhesion between the substrate surface and the coating deposited in the next steps of the process. In contrast, selective removal is known as *plasma dry etching process*, and is used, e.g., in the manufacturing of semiconductors. Conventional chemical etching, cleaning and solvent degreasing tend to leave pits or residual traces of process chemicals on the treated surface, whereas plasma-based cleaning and etching processes eliminate this drawback.

Although much of the industrial surface processing by plasma is performed in high- or ultrahigh-vacuum conditions as a consequence of the quality requirements for the final coating or surface properties, there are many plasma processes performed at pressures close to atmospheric levels, referred as Atmospheric Pressure Plasma (APP). These types

may be used for the generation of free radicals, e.g. O_3 [10], the emission of UV or Vacuum-Ultraviolet (VUV) photons (e.g. for microbial disinfection [11]), the decomposition of hazardous or toxic compounds, e.g. NO_X, SiO_2, or surface activation, to name just a few applications [12, 13]. The main advantage of APP over PVD methods is that it takes place at ambient pressure, which makes it possible to eliminate the high cost of a vacuum chamber and its associated components.

In the next section, we present a short description of each type of plasma process routinely used in industry.

1.1.1 Chemical Vapor Deposition (CVD)

Chemical Vapor Deposition is a group of deposition methods where a coating is formed from chemical constituents reacting in the vapor phase near or on a heated surface. The basic form of CVD is a thermal chemical vapor deposition, also called a vapor plating, where a precursor species containing the material to be deposited, are vaporized by the application of a high-temperature source. The vaporized precursor species reacts with other gaseous species present inside a vacuum system to form compounds (e.g. oxides, nitrides). Depending on the technical aspects of the process, various modifications of CVD methods are available, such as: Vapor Phase Epitaxy (VPE), used for single crystal film deposition [14]; Plasma-Enhanced Chemical Vapor Deposition (PECVD) or Plasma-Assisted Chemical Vapor Deposition (PACVD), where plasma is used to induce or accelerate the decomposition or reaction factor of a material [15], Low Pressure Chemical Vapor Deposition (LPCVD) [16], for processes that do not require vacuum conditions as high as those in VPE; and Metal-Organic Chemical Vapor Deposition (MOCVD), where the precursor gas is a metal-organic compound [17]. The main advantage of PACVD/PECVD over thermal CVD is reducing the activation temperature of the chemical reactions from above $700°C$, down to $300°C - 500°C$.

Although CVD and PECVD are mostly used for film deposition (e.g. in Liquid Crystal Display (LCD) manufacturing [18]), they can also be used for the removal of a coating from a surface in the dry etching process. The plasma sources used for chemical etching

are similar to those used for plasma-enhanced chemical vapor deposition. Precursor gases for chemical etching are selected such as will chemically react with the layer to be etched. An excellent example is NF_3 which, after decomposition in plasma, releases highly reactive fluorine radicals and ionized fluorine compounds that react with Si or SiO_2, thus removing it from the wafer. The resulting compounds are removed from the process chamber by a pumping system and, due to their toxicity, are then decomposed to environmentally safe products in a plasma-assisted *gas abatement* process [19].

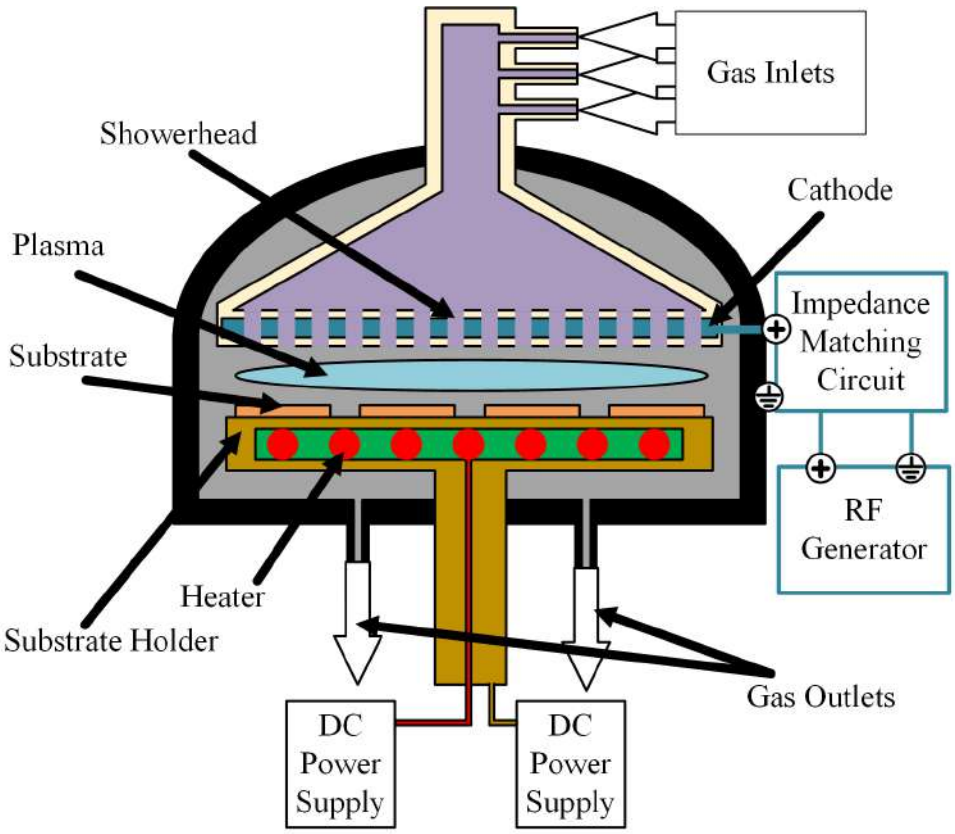


Figure 1. Simplified cross section of typical plasma chamber for a Plasma-Enhanced Chemical Vapor Deposition (PECVD) process [20].

Furthermore, physical and chemical etching processes can also be combined in the form of a Reactive Ion Etching (RIE) process – of key importance in the manufacturing of semiconductors [21]. This method combines ion bombardment of a negatively biased substrate (Si wafer) – which leads to the removal of the silicon – with the chemical etching of the film. Such a process therefore requires at least two power supplies: one

for the plasma source where the ions and reactive radicals are formed, and another to negatively polarize (bias) the substrate to attract and accelerate ions to the surface being etched away. Because this technique makes it possible to etch structures of a High Aspect Ratio (HAR), it is widely used in the semiconductor industry: from Through-Silicon Via (TSV) manufacturing [22], through nanocarbon film etching [23], up to GaN and Si surface treatment [24, 25].

A schematic view of a PECVD vacuum system is presented in Fig. 1. In particular, this is an Inductively Coupled Plasma (ICP) system geometry where the plasma is generated by a coil surrounding the cylindrical dielectric wall of the source region. Process gases are injected into the chamber through the source region and the plasma expands from there into the processing chamber, where the substrate is located. The ICP coil is supplied by an RF generator (i.e. 13.56 MHz), while the substrate, the material whose surface properties are to be modified, is placed on the substrate holder equipped with heaters, wafer cooling, sensors (e.g. temperature), and reference markers for the substrate positioning system. Further, the substrate holder permits the application of a bias voltage to the substrate using an RF power supply with the same or a lower frequency than that of the plasma source. Depending on the design, the substrate holder can be also connected to an additional DC power supply to apply high-voltage pulses in order to generate an electrostatic potential on the substrate holder surface for wafer positioning.

1.1.2 Physical Vapor Deposition (PVD)

PVD is an extensive group of deposition processes in which a source material (called also a target) is vaporized and the vapor is then settled on a substrate to form a coating. Depending on the desired properties and composition of the deposited film, the process may require the use of single or multiple targets, each of which may consist of one or more elements.

PVD techniques can be distinguished by how the source material vapors are produced. In evaporation, the target is heated up to its melting point to release particles of the source material into the processing chamber [26]. Alternatively, the target material

may be vaporized using a beam of high-energy electrons or ions [27]. In the case of magnetron sputtering, the target is eroded by bombardment with energetic ions. In both evaporation and sputtering, the next step is similar – the released target particles settle on the substrate. Additionally, if the target particles are ionized, a high electric potential may be applied to the substrate in order to accelerate the incoming ions and increase the density of the growing film. This procedure is called *substrate biasing*, and is further discussed in section 1.2.

The main advantage of sputtering over evaporation is the higher energy of the released target particles, used to increase the density of the coating and thereby improve its properties. Each PVD method sets different requirements for the power converters used in the plasma process. As an example, in the evaporation process, a simple DC current source can be applied, while for magnetron sputtering a variety of power supplies are used routinely in the industry due to the complexity of various applications.

In physical dry etching or plasma cleaning, as mentioned above, the kinetic energy of the accelerated ions is used to remove layers from the surface. Typically, such a process uses argon as the working gas. Argon ions available in the plasma are accelerated in a high electrical field introduced by the bias power supply. The proper adjustment of the negative voltage amplitude and process gas composition allows for precise control over the thickness of the layer removed.

A model of a typical process chamber used for magnetron sputtering is shown schematically in Fig. 2, while a detailed description of the magnetron sputtering process can be found in monograph [28]. Here only a basic description will be given of the working environment of a power converter used for plasma processing. To ensure the required processing conditions and to avoid impurities, plasma processes are usually performed in a vacuum or a low-pressure environment. For example, in the case of the magnetron sputtering, after the air is pumped out, the process chamber is filled with an inert gas such as argon. The power converter, e.g. a Pulsed DC power supply, is connected to the target (cathode) and to the chamber walls (anode), to provide the necessary energy to ignite and sustain the plasma discharge. Behind the target, a magnetron is placed to „trap”

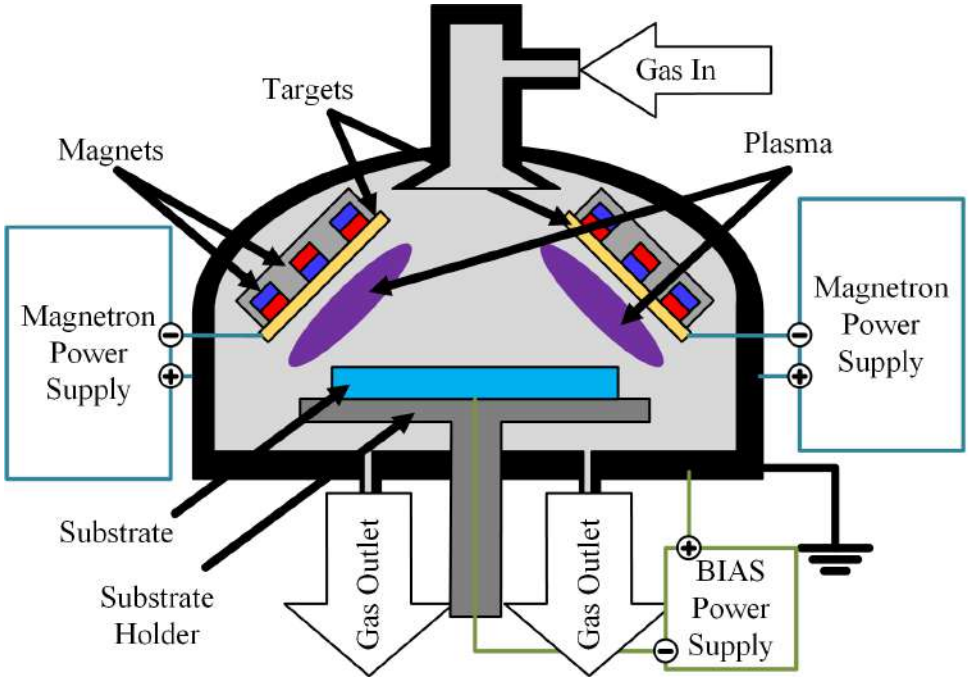


Figure 2. Simplified cross section of plasma chamber for a Physical Vapor Deposition (PVD) process [20].

electrons in the vicinity of the target and to increase the ionization of the inert gas in this area. The ionization process initially requires electrons. The electric field generated by the power supply accelerates the electrons towards the anode, and gas ions towards the cathode. Collisions of atoms with each other and with the electrons initiate a snowball process of ionization. When ions hit the target surface, their kinetic energy is transferred to atoms on the surface. If that energy is sufficient, the atomic bonds are broken and the target atoms are ejected from the surface. Due to the collisions, secondary electrons are also emitted from the target. Before reaching the surface on which the film is grown, the target atoms can be ionized or excited by collisions with plasma particles.

In many cases, a magnetron sputtering process involves using a second power supply connected to the substrate on which the film is deposited. Depending on whether the substrate is electrically conductive or not, a DC, Pulsed DC, or RF power supply is used as the bias source. The application of a negative potential (with respect to the grounded chamber wall) provides additional kinetic energy to the ionized target material. This excess energy is beneficial to the density and morphology of the deposited film.

A specific kind of PVD process is that of High Power Impulse Magnetron Sputtering (HiPIMS). In this process, short ($10 - 100\ \mu s$) impulses having a very high peak power ($0.5 - 6\ MW$) are delivered to a standard magnetron target, while the average power delivered to the target is kept at a level typical for magnetron sputtering processes (up to 60 kW). The high pulse power permits a high ionization of the sputtered material (up to 90%), and for this reason the method is widely used for the deposition of high-density, durable industrial coatings [29] including Diamond-Like Carbon films [30], deep trench filling and TSV structures in the semiconductor industry [31].

1.1.3 Atmospheric Pressure Plasma (APP)

Atmospheric Pressure Plasma (APP) overcomes one of the drawbacks of the above-described methods – operation in a vacuum. A process that can take place at ambient pressure eliminates the high cost of a vacuum chamber and its associated components. However, the difficulty of sustaining a glow discharge under atmospheric pressure conditions leads to a challenge, namely, the higher voltages required for the gas breakdown and arcing that occurs between the electrodes. Atmospheric pressure plasma processes can be classified by their electrode configuration, further discussed in [32]:

- Dielectric Barrier Discharge (DBD),
- Corona Discharge (CD),
- Plasma Jet (PJ) or Plasma Torch (PT).

DBD is generated between two electrodes where at least one is covered by a dielectric material. Thus, the plasma formed in the working gas fills the whole space between the positive and the negative electrode. Depending on the operating conditions, including the working gas composition, applied voltage and the frequency thereof, a filamentary or glow discharge will dominate. A filamentary discharge is formed by micro-discharges or streamers that develop on the dielectric layer surface. The dielectric layer plays an important role, as it limits the discharge current, thus avoiding a spontaneous transition from a glow discharge to an arc discharge. It is also responsible for the accumulation of electrons, and therefore for the statistically randomized distribution of streamers. Both

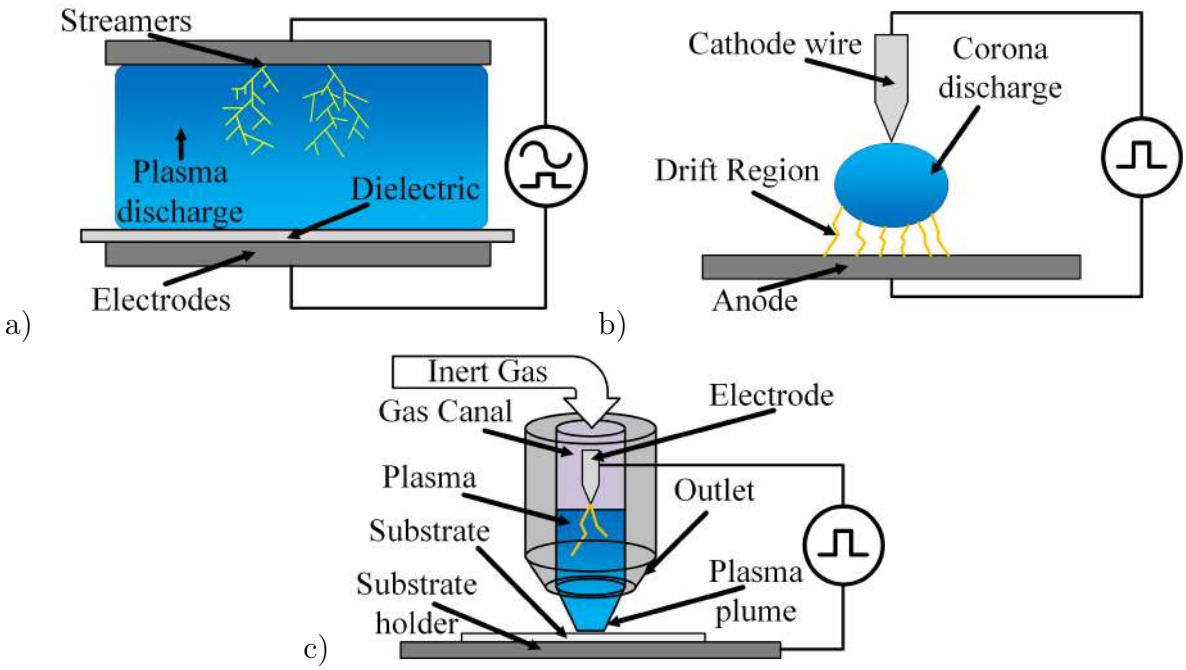


Figure 3. Atmospheric plasma: a) Dielectric Barrier Discharge (DBD), b) Corona Discharge (CD) and c) Plasma Jet (PJ) [20, 33].

the distance between the electrodes and their geometry depend on the operating conditions (especially the gas mixture and voltage) and vary from micrometers to a few centimeters.

A CD is a luminous glow around the sharp tip of a conductor, formed by the ionization of the surrounding gas in a highly non-uniform electric field. It occurs when the potential gradient at the sharp tip exceeds a threshold value, but is not sufficient to cause a complete electrical breakdown. CD is unwanted and dangerous phenomenon in high-voltage systems, but it is used in many industrial applications such as Electrostatic Precipitator (ESP), which was developed to remove sulfuric acid fumes from a gas stream. ESPs are used in such processes as the manufacturing of steel, paper and cement, as well as in ore-processing industries and as combustion sources in power plants for collecting particulate emissions [34].

Finally, a characteristic feature of PJ and PT is that the plasma is ignited and sustained within the plasma source, but extends beyond the region where it is generated, and is launched outside the device in the form of what is known as a "plasma plume". Despite the large variety of configurations, almost all plasma jets structurally integrate an electrode

assembly for the generation of the discharge and a channel through which the working gas flows and in which the plasma generates and propagates. Usually the channel has a circular (or round) cross section perpendicular to the direction of the gas flow [33], although ring-shaped or rectangular geometries are also used. The ionized gas from the plasma jet is directed onto a substrate a few millimeters downstream. As the temperature of the ionized gas is low (below $180°C - 200°C$) it can be used to etch materials such as plastics or silicon dioxide, as well as in various medical applications including plasma-assisted tissue coagulation and dissection [35, 36].

Since DBD, CD, and PJ sources all differ in their construction, the voltage and power needed in them to ignite and sustain the discharge also vary. CD typically requires a higher voltage of several tens of kilovolts, while DBD typically operates at a lower voltage and power. In contrast, PJ and PT benefit from a discharge ignition voltage in the range of those used in magnetron sputtering, below 1 kV.

1.1.4 Plasma systems

As it was stated at the very beginning of chapter 1, plasma processing techniques are used to manufacture various of every day objects. What has not been properly pointed out yet, is the complexity of manufacturing processes. The path from the intermediate goods to the final product - e.g. camera lens or LCD screen - consists of tens or hundreds of different steps, which mostly requires usage of HPPS. One of the best examples to visualise this aspect of plasma processing, are semiconductor chips. In fact, design of integrated circuits is similar to the Printed Circuit Board (PCB), although the dimensions of the first ones are few order smaller and the amount of layers is significantly higher.

The first step is preparation of silicon substrate. For this purpose, the high purity polysilicon cylinder is placed inside vacuum chamber. Then, inductive heating coil heats up part of cylinder up to the ($1400°C$), which causes the impurities to gather on the surface. The heating coil is moved along cylinder, to concentrate impurities at the very end of cylinder where they are cut off. At last, cylinder is cut into wafers, which are further covered with thin film of SiO_2, for protection from undesired oxidation and contamination.

Inductive heating, mentioned in this paragraph, is one of many applications of modern HPPSs.

Next, wafers are subjected to photolithography, etching and doping. The oxidized silicon wafers are uniformly covered with a photoresist material. Such prepared wafer is further exposed to the UV light through proper photomask, which stops the UV beam and allows to transfer complex geometric design onto silicon surface. The exposed areas of the chip pattern are removed, revealing SiO_2 surface below, while areas protected from the UV irradiation remains intact. Afterwards, exposed SiO_2 patterns are etched off during either chemical or plasma etching process. Remains of photoresist layer are chemically removed and processed wafer is subjected to further chemical or plasma cleaning. Such prepared wafer is subjected to oxidation process, to develop an insulating layer, on top of which a conductive layer of polysilicon is deposited. Next, stack-up is covered with photoresist material, which is again exposed for the UV irradiation through proper photomask and etched, to remove deposited polysilicon and insulating oxide layer from desired areas of wafer. At last, the exposed silicon areas are subjected to the ion implantation process to dope Si with B or P, and to develop p and n regions respectively. Afterwards, wafer is subjected to another cycle of oxide layer deposition, applying of the photoresist, UV irradiation and stripping. Then, to develop contact with underlying layers, the conductive metallic alloys are deposited. These steps are then repeated few-dozens or few-hundred times, until stack-up is completed. This stage of manufacturing heavily relies on HPPSs, which are used to:

- supply UV lasers,
- supply ion sources,
- deposit silicon and metallic layers in PVD process,
- etch semiconductor wafer.

If any of these steps is interrupted, e.g. due to a failure or a unscheduled shutdown of plasma system, the whole batch of processed wafers is wasted.

Production of semiconductor devices is a great example of a batch system, designed to process specified amount of devices at once. Other great example of such application

is manufacturing of Flat Panel Displays (FPD), where a single glass panel - varying from 1300 x 1500 mm to 2940 x 3370 mm depending on system generation - is processed at once [18]. The alternate approach for plasma processing is presented by the in-line systems. In such system, production line is constantly supplied with steady stream of intermediate good, which is moved along series of vacuum systems, each operating 24/7 and optimized for distinct type of plasma process.

Typical application of in-line plasma systems is low-E glass manufacturing. At first, glass panel goes into pressure cleaner to degrease it and remove all pollutions. Next, it is dried and goes into series of vacuum chambers, each with lower pressure than the previous one. Such concept is in fact similar to the operation principle of the water gate. At last, when pressure is decreased to few $mTorr$, glass goes into target plasma chamber for sputtering. After deposition of multiple layers of Ti, Ag, TiO, ZnO and other compounds, glass panel leaves plasma chamber and goes for the quality control.

Same as in the case of semiconductor device manufacturing, each unplanned shutdown or interruption may deteriorate quality of deposited layer, resulting in high financial and material losses. In contrast to the batch system, material wastes are not be limited to the volume of single batch, as production line is constantly supplied with the intermediate good.

High complexity of plasma processes causes very high complexity of the manufacturing equipment iself, with a great example of Extreme Ultraviolet (EUV) lithography machine. As presented in [37, 38], such systems consists of thousands of non-redundant parts, which implies an extremely high reliability requirements for each component used in it.

1.2 Power supplies for plasma applications

Depending on the application, the maximum average power delivered to plasma ranges from a few watts (e.g. a plasma jet for wound disinfection in medical applications) to more than a hundred kilowatts from a single power supply unit (e.g. large-scale glass coating systems). Moreover, power supplies for industrial plasma material processing applications differ in their control concept, shape and fundamental frequency of output signal or peak

output current, depending on the target application. In this section, main types of HPPSs and power converter topologies suitable for such applications are discussed.

1.2.1 Taxonomy

There are two main approaches to categorize power supplies for plasma processes: by their application or by the shape of their output voltage and current. In the first case, HPPSs are divided into the following groups:

- Bias sources,
- Plasma sources (e.g. magnetron, ion sources).

Bias sources are used to introduce a negative DC offset between the substrate and the reference electrode, typically the chamber walls at the ground potential, in order to accelerate ions from the plasma to the substrate. This feature is commonly used to increase the film density and deposition rate in thin-film growth; to decrease the roughness of a sputtered film, or to increase the etch depth in semiconductor manufacturing [39–41]. In general, DC or Pulsed DC Bias sources are mainly used where electrically conductive substrates feature. In such cases, the power converter has to act as a nearly ideal voltage source, with voltage ripples of less than 1% in order to increase the homogeneity of the electrical field, which is essential for growing high quality, uniform films. For more challenging dielectric substrates, it is possible to exploit the plasma's self-bias property and introduce a precisely controlled bias voltage with an RF power generator.

Power supplies used as plasma sources (e.g. magnetron sources, arc sources, ion beam sources, etc.) have to act as a nearly ideal current source. Key features of such power supplies are their ability to shut down output current in microseconds and to suppress arcing. The generic root cause of arcing is poisoning – the growth of a dielectric layer on the target surface or the surface of the biased substrate. As the plasma process goes on, a thin insulating layer made of a compound of the target material (such as Al) and the process gas (such as O_2) is deposited on the target surface. A dielectric film is typically sputtered (or removed from the target surface) more slowly than a pure metal, and accumulates an electric charge. As the electric field across the dielectric film

increases, any local distortion of the electric field can lead to an uncontrolled discharge – an arc. Moreover, an untreated arc can seriously damage the target, leading to an abrupt, unplanned stoppage of the production process for target maintenance.

If power supplies for plasma applications are categorized by the shape of their output voltage or current, and their fundamental frequency, as in Fig. 4, the following groups emerge:

1. Direct Current (DC) sources,
2. Pulsed Direct Current (Pulsed DC) sources,
3. Medium Frequency (MF) and Bipolar sources,
4. Radio Frequency (RF) and Very High Frequency (VHF) sources.

DC power supplies have a broad range of applications. They provide a constant, low-ripple current (in plasma source applications) or voltage (in bias source applications), and are used for substrate heating, electrostatic chucks for wafer positioning, high-voltage sources for atmospheric plasma discharges, and in many other applications.

Pulsed DC power supplies are also used as plasma and bias sources. The main difference between a Pulsed DC and a DC power supply is the ability of a Pulsed DC supply to perform a fast ON and OFF sequence, so as to produce rectangular waveforms of output voltage and current. The application of pulsing and a regulated duty cycle is used to minimize the probability of arcing due to the target poisoning. In a Pulsed DC sputtering process, a short off-time allows for the neutralization of the positive charge accumulated on the surface, covered with the dielectric film during the on-time. The efficiency of mitigating arcing by Pulsed DC can be further increased by the application of a so-called *reverse voltage*. The above-mentioned benefits of pulsing and reverse voltage are also utilized in bias applications of Pulsed DC power supplies.

Another group of power converters for plasma processing applications is that of Medium Frequency sources. Low-power supplies are used, e.g., for solar panel manufacturing, while 120 kW generators find application in large-scale systems for architectural glass coating. The main difference between MF/Bipolar and other types of plasma power

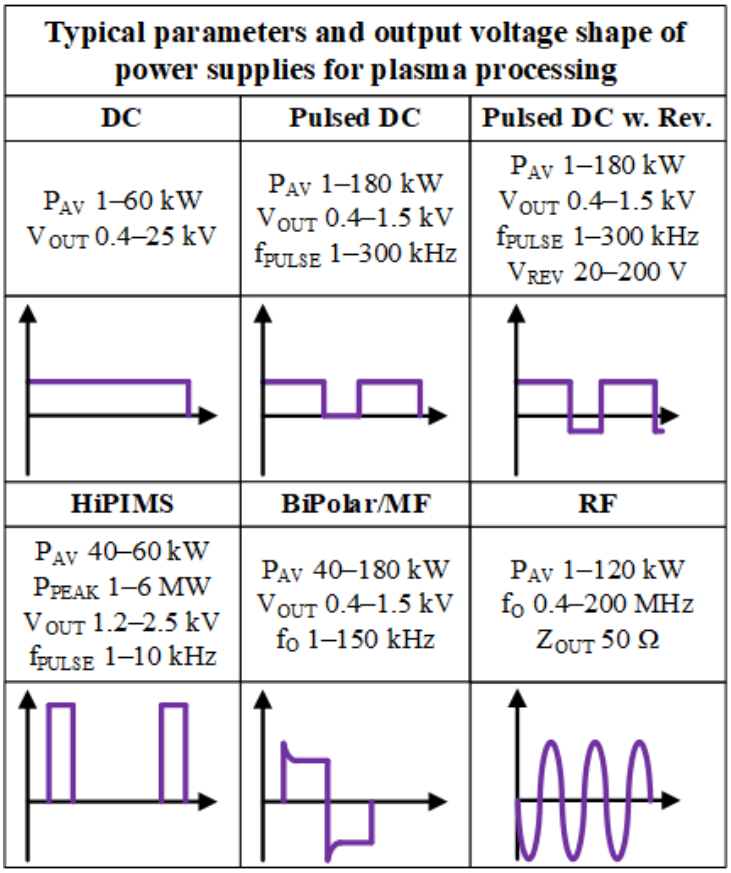


Figure 4. Main types of High Performance Power Supplies (HPPSs) for plasma processing [20]. Critical parameters of HPPSs are: Average Output Power (P_{AV}), Output Voltage (V_{OUT}), Pulse Frequency (f_{PULSE}), Amplitude of Reverse Voltage (V_{REV}), Peak Instantaneous Output Power (P_{PEAK}), Main Output Frequency (f_O) and Output Impedance (Z_{OUT}).

supplies is their design; they have two independent output terminals, which may or may not be electrically grounded. Therefore, in the magnetron sputtering applications they are typically used in a dual magnetron arrangement, where both output terminals are detached from the electrical ground. Such an electrical configuration results in the target alternately functioning as cathode and anode, depending on the actual polarization of each of the power supplies' output terminals: when one of the outputs is polarized negatively to perform sputtering, the other one is acting as the anode. After one half-period, the electrical conditions are reversed, and the first target is now the anode, while the sputtering process continues on the second target.

The next main difference between Medium Frequency (MF) and Bipoler power supplies is the shape of output voltage and current. MFs provide an alternating sine-wave output

signal, while in the case of Bipolar units, the shape of the output signal can be modified to achieve a rectangular, triangular or trapezoidal waveform. The ability to modify the current and voltage waveform shape during normal operation, without additional mechanical changes, makes it possible to manipulate the average plasma ion energy, which is essential for the deposition of oxygen-based films (e.g. SiO_X, ZnO_X, GaO_X) [42], as in these applications, too high a kinetic energy of O^- ions may result in an undesired damage to the deposited film [43].

The last major group of power supplies used for plasma processing are RF and VHF power supplies. In particular, 13.56 MHz and its harmonics are the most typical operation frequencies reserved for industrial and medical applications. Depending on the application, RF power can be generated by applying an RF voltage across two parallel electrodes installed in a vacuum chamber Capacitively Coupled Plasma (CCP) or by circulating RF currents in a coil mounted on the outside of the vacuum chamber and separated from the plasma by a dielectric window ICP. Both methods transfer the energy of the RF electromagnetic wave to the electrons in the plasma to sustain the discharge.

1.2.2 Power converters topologies

Power supplies for plasma processing applications are usually complex, modular systems with multiple stages of the energy conversion, as presented in Fig. 5. Various types of power converters may be found suitable to be used in such power supplies but in different plasma processing applications. Therefore, any comparative study of the basic types of power converters should take account of the potential usage of these topologies in the same functional module of the HPPS for the plasma processing application. Therefore, the following assessment method is proposed – each type of power converter can be identified as:

- well suitable,
- suitable,
- not suitable,

for following target application:

- input stage of HPPS for plasma processing,
- interlink stage of HPPS for plasma processing,
- output stage of HPPS for plasma processing.

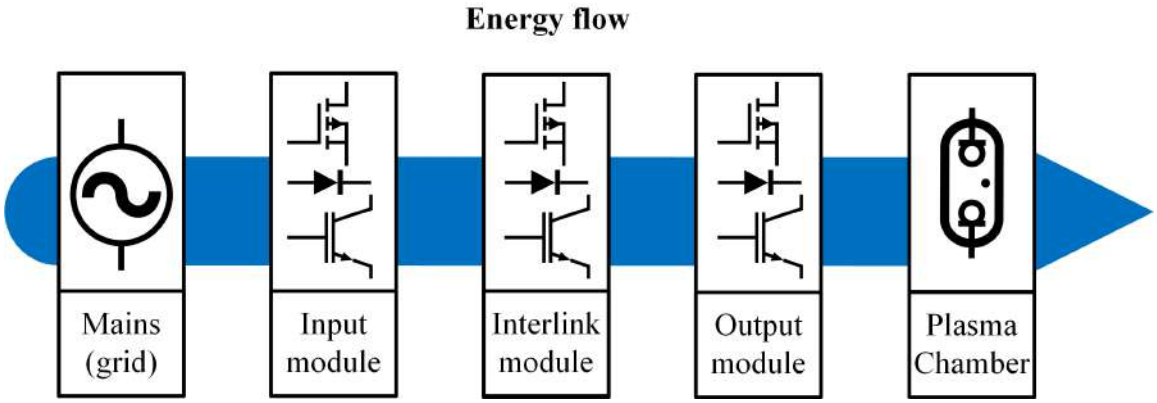


Figure 5. Simplified block diagram of a typical power supply for plasma processing with energy flow direction marked [20].

Typical Key Performance Indicators (KPI) used for comparing various designs of input modules are:

1. Current Total Harmonic Distortion (THDi) on input terminals,
2. Voltage Total Harmonic Distortion (THDu) on input terminals,
3. power factor,
4. efficiency,
5. total cost.

However, in the plasma surface processing applications, these KPI are insufficient, and two additional indicators have to be defined:

7. main frequency power fluctuations seen at the output of the power supply,
8. immunity for pulsed operating conditions [44].

Indicators 1. - 5. are rather typical for all power electronic equipment, as they are fundamental for power quality improvement and economic evaluation. However, the strict

limits on the presence of the mains frequency in the output signal are unique to the plasma processing. Low-frequency fluctuations disqualify a power supply's design from bias applications because these impact the plasma properties, including the ion energy density, which can lead to a deterioration in the quality of the coating.

A typical design of an input module is a simple bridge rectifier with a unidirectional boost converter, as presented in [45, 46], although other hard-switching converters (e.g. interleaved boost converter [47] or a buck converter [48]) can also be successfully utilized. Moreover, various researchers have proved that resonant converters (e.g. LLC, LCC) can also be used in such configuration [49], although the design of a wide input range resonant converter, which is immune to voltage sags and other grid events, is far more challenging than in the case of a hard-switching topology. Thus, in the scope of a wide-range operation, a non-inverting buck-boost or Single-Ended Primary Inductor Converter (SEPIC) topology [50] outperforms other converters, as it can provide either a higher or a lower voltage on the output terminals, than on input. Although typical buck-boost or Cuk converters also have similar properties, they invert the output voltage polarity, which can cause additional design issues. Recently, bridgeless designs (e.g. bridgeless boost, totem-pole Power Factor Correction (PFC) circuit, bidirectional boost converter, active bridge [51, 52]) have become increasingly popular in industrial and automotive applications [53], for being more efficient than bridge-based solutions, achieving rates of $97.5\% - 99\%$ [54, 55]. Moreover, an improvement in efficiency has been proved for both single-phase and three-phase designs [53, 56]. An active bridge topology stands out among the above-mentioned designs in terms of KPI 1. and 2., as state-of-the-art control algorithms (e.g. space vector modulation [57]) permit a significant reduction in either current or voltage total harmonic distortion. On the other hand, active bridge and totem-pole designs require far more active components than bridge-based input models.

Various researchers have proved that a single-stage LLC resonant converter [58, 59], an LCC resonant converter [60, 61], a semi-soft switching converter [62, 63], or a hard switching converter [46] are well suited as intermediary power conversion systems. Therefore, these types of power converters could be easily adapted for the purposes of

forming an interlink for every type of power supply for plasma processing. Although modular or multilevel converters [64, 65] can also be successfully utilized as an interlink in any plasma power supply, such power converters are better suited to HV applications, as using a multilevel converter in a low-voltage source may prove to be sub-optimal in terms of Design to Cost (DtC) [66] or DfR [67] methodology. However, in some designs, the input and interlink modules are combined into a single functional module. Then, performance evaluation should focus on the KPI defined for input modules.

As shown in Fig. 4, almost every power converter topology is applicable at the output stage of a DC power supply, however no topology is universal, nor is any solution suitable for every application. Therefore, any decision on the design of a DC power supply for plasma processing should be supported with a detailed analysis of the functional requirements and the power supply application. As an example, a resonant converter (e.g. LLC or LCC) is a good choice for a highly efficient device with a rather narrow linear control range, as in the case of a power supply for resistive heating in epitaxial crystal growth. On the other hand, it would perform poorly as a plasma source with a wide range of linear output voltage and current regulation. For the same reason, resonant converters are inadequate for bias power supplies, because such a topology is not optimal for idle work, typical of bias applications. The bias power supplies usually operate with a high output voltage but very low current.

As in the case of an interlink, multilevel converters are a good choice for a high-voltage application (e.g. CD, DBD), while using such a topology in a low-voltage application (e.g. arc sputtering, arc welding [46, 64]) could be simply inadequate. Here, a single-stage hard-switching power converter is often an appropriate solution [68].

In the case of a Pulsed DC power supply, the device architecture has to be able to shut off the voltage and current within microseconds to achieve a „rectangular" signal shape. Therefore, the output stage of such a power supply needs to have either a very low output capacitance [69] or the ability to short both output terminals with a controlled electronic switch [70, 71]; this favors topologies such as, e.g., a synchronous buck converter. For

better clarification, a comparison of the output stages of a simple DC and a Pulsed DC power supply for plasma processing is presented in Fig. 6.

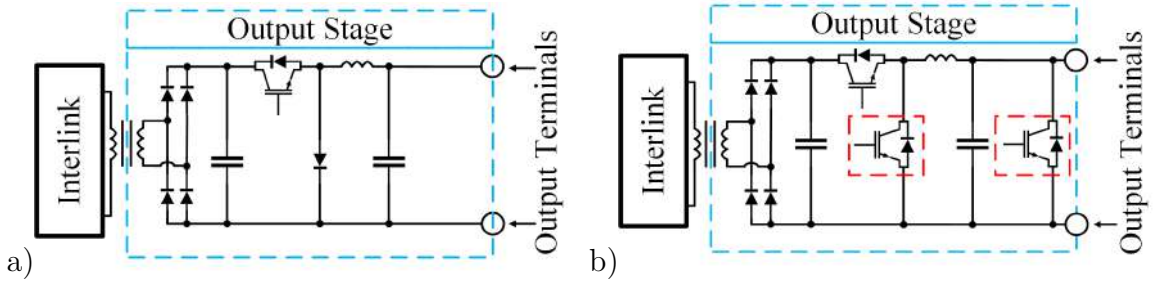


Figure 6. Comparison of output stage for a Direct Current (DC) plasma source for magnetron sputtering [72] (a) and a Pulsed Direct Current (Pulsed DC) bias source for a Chemical Vapor Deposition (CVD) system [71] (b). A typical configuration of the electronic switch shorting output terminals is marked with a red dashed line [20].

Sample voltage and current waveforms of a DC and a Pulsed DC power supply are presented in Fig. 7. To achieve such a high di/dt and du/dt slope, the power supply has to be able to extract the energy stored in the parasitic inductance of the cables connecting it to the cathode (the sputtering target). For this purpose, a slightly negative voltage may be introduced at the end of each pulse [73], as presented in Fig. 7b).

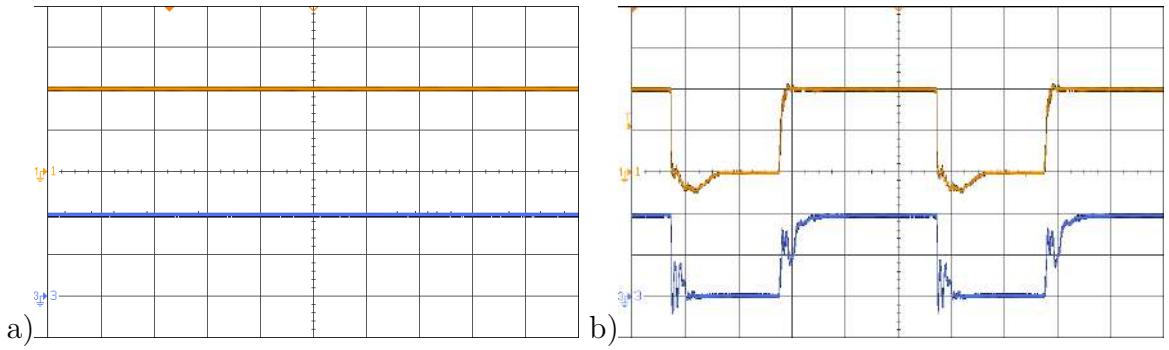


Figure 7. Output voltage (yellow, upper) and current (blue, lower) of 20 kW bias power supply in a Direct Current (DC) mode a) and Pulsed Direct Current (Pulsed DC) mode b). Timescale - 50 $\mu s/div$, channel 1 - 200 V/div, channel 3 - 5 A/div [20]. Black line is a ground level (0 V).

The choices become much more limited for Bipolar and MF supplies, or Pulsed DC supplies with Reverse Voltage, since such devices:

- need to be able to operate with both output terminals separated from the electric ground,

- need to deliver both positive and negative voltage between terminals.

Therefore, transformer-based power converters, half-bridge converters, full-bridge converters and multilevel converters perform better in such applications, as has been clearly demonstrated by various researchers – [59, 74–77]. If necessary, Reverse Voltage can be also introduced by interrupting the current flowing through the choke, as is presented in [78, 79]. Unfortunately, such a solution has a significant disadvantage – the amplitude of the Reverse Voltage is a product of the current flowing through the choke, which is dependent on the load impedance and on-time, and is therefore uncontrolled. Here, a transformer-based design or multilevel converter makes it possible to achieve an easily controlled, rectangular shape of reverse voltage, as shown in Fig. 8. Examples of typical solutions for the output stage of Bipolar or Pulsed DC power supplies with Reverse voltage are presented in Fig. 9.

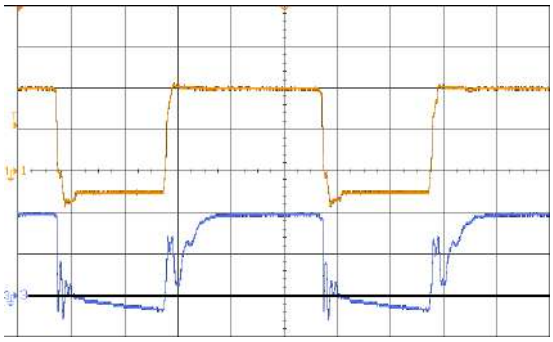


Figure 8. Output voltage (yellow, upper) and current (blue, lower) of 20 kW bias Pulsed Direct Current (Pulsed DC) power supply with Reverse. Timescale - 10 $\mu s/div$, channel 3 - 200 V/div [20].

In the case of HiPIMS, the power supply has to deliver extremely high power to the cathode in a very short pulse. For such a high current and voltage rating (approximately 1000 A and 2000 V), multilevel and modular converters seem to be the best choice, as they make it possible to keep the voltage, current, and power rating across either electronic switches and passive components at a reasonable level. Moreover, a multilevel and modular approach allows the use of mature, proven components rather than experimental technology, which is critical from the point of view of reliability-oriented design. In an HiPIMS application, a cascaded connection of multiple isolated

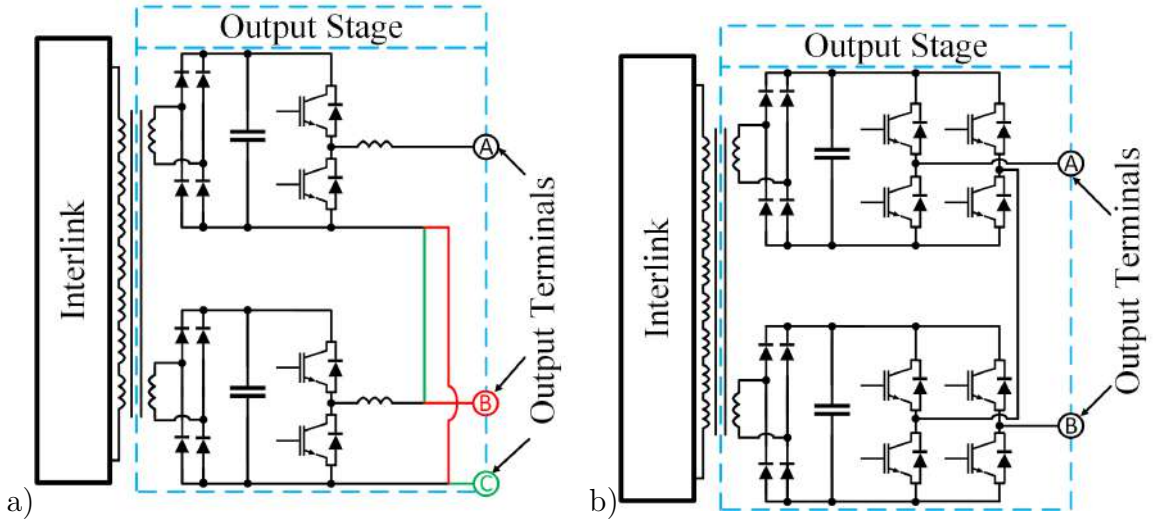


Figure 9. Comparison of output stage for Pulsed Direct Current (Pulsed DC) plasma source with reverse voltage a) and Bipolar plasma source [74] b). There are two typical configurations of output terminals for power supplies with Reverse voltage: $A - B$, marked with black-red line [77] and $A - C$, marked with black-green line [20, 75].

DC sources (e.g. a cascaded H-Bridge [74]) is the best solution, as it allows for a wide-span output voltage/current control and a sharp voltage slope formation, essential for plasma processing. A similar approach is presented in [80], where a cascaded connection of multiple buck converters was utilized to develop a pulse power supply for high-energy lasers.

Last but not least, due to the very high operating frequency of RF power supplies ($0.4 - 200\ MHz$) only soft- or semi-soft switching power converters can be successfully employed. Typical power amplifier classes suitable for plasma processing applications are AB, D, DE, E, F^{-1}, although the AB class is rarely seen nowadays due to its rather low efficiency (up to 70%) [81–85]. In contrast, the rest of the above-mentioned power amplifier classes allow for nearly 95% efficiency while maintaining satisfactory spectral purity of the output voltage waveform. As was stated above, a key feature of every power supply for plasma processing applications is their ability to ignite the plasma. In the case of RF and VHF power supplies, to fulfill the above requirement, the voltage amplifier has to be able to withstand operating under a heavily mismatched load, since the process chamber represents an open circuit before plasma ignition. Therefore, the typical Voltage Standing Wave Ratio (VSWR) for this type of power supply is specified as being from

~ 2.62 for nominal operating conditions up to ~ 25 for plasma ignition conditions, and must be achieved with limited power in a short time period. The power converters most commonly used in the output stage of RF and VHF power supplies are presented in Fig. 10.

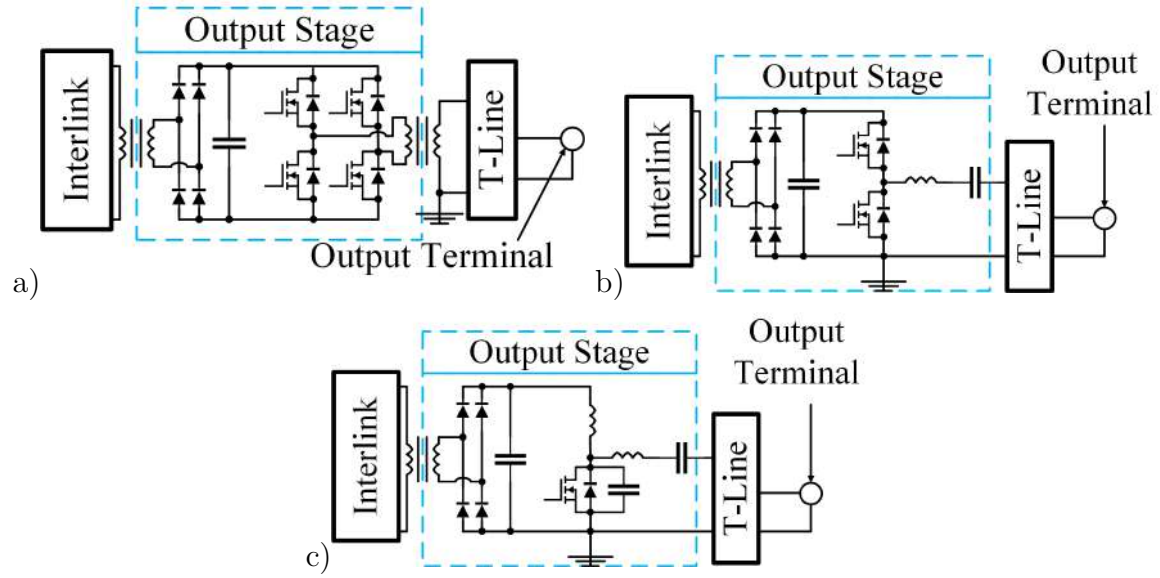


Figure 10. Typical resonant converters used in Radio Frequency (RF) power supplies for plasma processing [86] (a) class D [84], (b) class DE (modified D) [83] and (c) class E amplifier [87].

1.3 Conclusions

Analysis presented in this chapter shows variety of plasma processing techniques, and their applications in modern industry. Such broad scope of processes simply can not be covered with only one type of power supply. Thus, HPPSs are in a fact a broad family of diverse power converters, starting from simple hard-switching converters, up to sophisticated high frequency amplifiers. Although they have a very distinct differences in their design, most of HPPSs are modular devices, with 2 or more levels of power conversion. Comparative evaluation and KPI-based analysis of common power converter topologies shows, which power converters can be considered as *preferable* for certain HPPSs. Next, many of HPPSs have to fulfill a very unique requirements, resulting from operation in plasma system - e.g. ability to withstand and suppress arc, supporting a very high du/dt at output voltage,

ability to withstand high VSWR and others. All these aspects indicates that HPPSs are extremely complex devices, consisting of multiple modules or critical components. Last but not least, increasing demands on power density of modern HPPSs drives their design to the limits.

Next, presented examples bring up a typical operating profiles, for which HPPSs are subjected to.In the case of batch systems, typical for e.g. semiconductor device manufacturing or flat panel display industry, HPPSs are subjected to severe power cycling, related to repetitive ON and OFF conditions, caused by repeating plasma process and technological breaks required to swap the batch. In contrast, in the case of in-line systems, HPPSs operates with nominal power for almost all the time.

At last, discussed examples production processes, showed not only great a complexity of a plasma processing techniques, but also their susceptibility for changes. Any malfunction or undesired shutdown of HPPS may deteriorate quality of processed layers, resulting in high financial losses, related to waste of processed intermediate good and time, spent on restoration of production line. This explains high reliability and quality requirements for all equipment used in plasma processing industry - especially for HPPSs.

All of these aspects explains the motivation behind the research presented in this paper, focused on increasing reliability of High Performance Power Supplies.

Chapter 2

Reliability improvement of High Performance Power Supplies (HPPSs)

The simplest definition of the reliability is a probability, that a device used in certain operating conditions, will keep its functionalities over a specified time [88]. Based on this definition, the reliability improvement of the HPPSs may be fulfilled by:

1. the fault-tolerant design, which allows to maintain main functionalities despite fatal failure of either single or multiple critical components,
2. the condition monitoring or Remaining Useful Lifetime (RUL) estimation, which allows to limit a probability of failure thanks to the preventive maintenance,
3. the reliability modelling, which ensures that failures will occur after desired time (e.g. a warranty period) or allows to introduce proper preventive maintenance strategy,
4. the reliability oriented design, which ensures that designed HPPS will meet desired reliability goals.

2.1 Cross comparison of different strategies for reliability improvement

The fault tolerant design concept is based on two foundations - the first is the redundancy of critical circuits, and the second one is the detection of faulty condition. Although redundancy may be introduced on switch-level, leg-level, module-level or system-level as depicted in Fig. 11, in every case the fault-handling algorithm is the same: after failure detection, power supply changes configuration of switches to isolate damaged semiconductor device, and then restores operation.

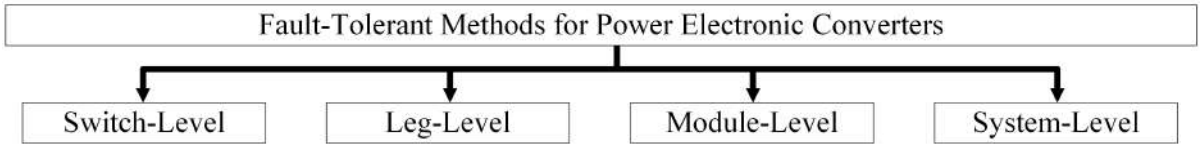


Figure 11. State-of-the-art fault-tolerant methodology chart - simplified view [89].

Although the fault-tolerant design is a very interesting concept, which is currently introduced for various applications, from renewable energy sources [90, 91], through electric propulsion systems in automotive industry [92], up to power electronic transformers [93] for grid applications, it may not be the best strategy for the HPPSs for plasma processing. The main disadvantage of any fault-tolerant design lies in its very foundation - a redundancy of critical circuits. This would not only increase a unit cost of HPPS, but also its size, which opposes to the market demands. Simply, power supplies for plasma processing has to be as small and as cheap as possible. At last, it is not sure if the fault-tolerant design is indeed a solution for problem stated in section 1.3. The fault-handling itself, which is an identification of a fault condition and reconfiguration of the power converter requires time, during which the energy flow to the plasma chamber will be distorted, which still may deteriorate quality of the processed layer. Thus, the fault-tolerant design may not be appropriate for certain applications, which are very susceptible for any changes or instabilities of process conditions, like semiconductor manufacturing.

In the case of either the condition monitoring or the RUL estimation, a overall reliability of the HPPS is increased thanks to detection of a progressing degradation,

which allows to prevent a failure. The reliability improvement strategy may be based on actual measurements of so-called *health indicators* [94, 95], simulation study and advanced electrothermal modelling or mix of both [96]. Depending on the chosen strategy, the State of Health (SoH) estimation may be performed on-line, if health indicators are recorded during normal operation of the power converter or off-line, if condition monitoring requires stopping the machine and performing of a dedicated check-up routine. Alternatively, SoH estimation methods may be categorized by the origin of data processing. The SoH estimation algorithm may be implemented in power converter itself [94, 97], or calculations may be performed on dedicated server, as presented in [98, 99]. In the second case, one of approaches worth mentioning is condition monitoring based on the machine learning [100, 101].

Although the SoH assessment for purposes of either the condition monitoring or the RUL estimation is a very interesting concept, it has some fundamental limitations. The first challenge related to the practical implementation of the SoH assessment, is the variety of critical components used in modern power converters. Power semiconductor devices, capacitors, integrated circuits, magnetic components, etc. - each of these components has its own unique degradation mechanisms. Thus, not only each type of critical component has its own health indicators, but also requires proper measurement method for the SoH assessment. Beside the *variety* of critical components, the *number* of critical components is also a challenge for practical implementation of condition monitoring procedures. As presented in [102, 103], useful health indicators monitoring often requires complex measurement or driver circuit. Although many researchers presented successful concepts of condition monitoring techniques for single functional modules (e.g. DC-link [104], Insulated Gate Bipolar Transistor (IGBT) module [98]), HPPS may consist of dozens of discrete semiconductor devices. This brings up concerns about scaling up of the SoH assessment strategy, especially for a very compact designs, typical for modern HPPS. Moreover, details of plasma process parameters, like power delivered to the plasma chamber, current, voltage, arc rate, operating frequency, Pulse On-time (t_{ON}), Pulse Off-time (t_{OFF}), etc. are usually a strictly protected know-how. Thus, the condition

monitoring which would require connecting with external server, brings up concerns about a cyber-security and safety of recorded data [105, 106].

The DfR is widely used to increase the reliability of either complex power electronic systems [107] or simple single-stage converters [108]. Similarly to the reliability modelling, it is based on the idea that overall reliability of the power converter can be estimated for predefined set of stressors, based on known reliability models for either functional modules (e.g. driver circuit) or critical components (e.g. power semiconductor device, capacitor). The distinct difference between these two concepts is their scope. The reliability modelling is used to estimate the reliability (e.g. failure rate, useful lifetime) of critical components, functional modules and whole power converters for given operating conditions, based on defined probabilistic models. In contrast, the DfR defines not only probabilistic models for reliability modelling, but also:

1. design rules,
2. guidelines for stress level estimation,
3. guidelines for useful lifetime calculation,
4. test procedures (e.g. for detection of possible design flaws),
5. accelerated lifetime test procedures (e.g. for reliability demonstration).

Thus, DfR (also known as *reliability oriented design*) is significantly more holistic approach, than the reliability modelling, as it covers multiple aspects of reliability engineering.

As depicted in Fig. 12, concepts of the DfR and the reliability modelling partially overlap. Thus, they share some of advantages and disadvantages in comparison to other strategies for reliability improvement. The main challenge with implementation of either of methods in real-life engineering workflow is accuracy and number of statistical models used in the reliability assessment, which may cause serious under- or overestimation. As it was mentioned earlier, each critical component of modern power converter is subjected to its own degradation and failure mechanisms. Moreover, often it is possible to distinct a few

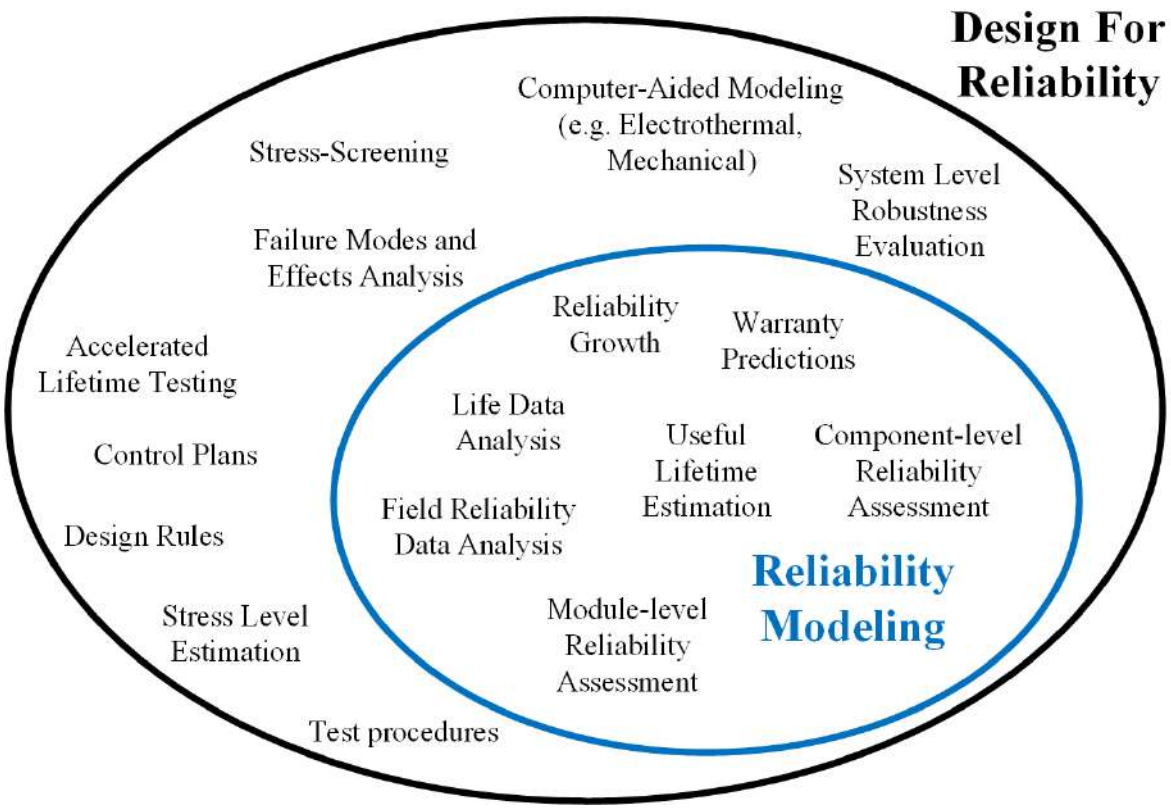


Figure 12. Graphical representation of the Design for Reliability (DfR) concept in comparison to the Reliability Modelling approach.

different failure modes, accelerated with different stressors, for each critical component. Thus, proper reliability assessment would require usage of multiple probabilistic models, each for separate failure mode. On the other hand, number of the same critical components (e.g. total amount of capacitors or power semiconductor devices) is not challenging at all, as proper calculations can be easily repeated. Next advantage of either the DfR or the reliability modelling strategy is easy scalability for modular devices, like HPPSs. Based on presented analysis, the DfR concept was found as the most suitable strategy for reliability improvement of HPPSs. Thus, a proper DfR procedure - suitable for needs of TRUMPF Huettinger Sp. z o.o. (TRUMPF) - was established.

2.2 Fundamentals of the Design for Reliability (DfR)

As presented at the beginning of Chapter 2, reliability is in fact a probability of success, defined as: correct operation of device after certain time, for given operating conditions. Thus, it is very common to use probabilistic and statistics measures to denote reliability. Either single device (e.g. semiconductor chip), functional module (e.g. control board) or whole system (e.g. power converter) might fail at any time. Thus, reliability has the characteristics of the continuous random variable. Alternate approach is to consider part/module/system as defective or non-defective. In such case, random variable – the reliability – can take only one of the two values. In this case, reliability is considered as a discrete random variable, similarly to probability of a coin toss. Thus, the probability of failure can be expressed with a probability density function or probability mass function, respectively to chosen approach. However, it is far more common to treat reliability as a continuous random variable, than discrete. Therefore, the mathematical apparatus typically used to denote probability are:

- Probability Density Function (PDF) - denoted as $f(x)$
- Cumulative Density Function (CDF) - denoted as $F(x)$

In the case of the reliability modeling, the PDF represents the relative frequency of failures as a function of time. By the definition, the CDF is the cumulative value of the PDF, thus in reliability modeling it represents the absolute probability of failure over time. Therefore, it is also known as the Unreliability Function ($Q(t)$), as it is used to measure the probability that part/module/system will fail before certain time. The graphical representation of the relationship between PDF and CDF is depicted in Fig. 13. As the probability can not be higher than 1, the Reliability Function ($R(t)$) can be defined with Eq. (1):

$$R(t) = 1 - Q(t) = 1 - \int_0^{\tau} f(t)dt = \int_{\tau}^{\infty} f(t)dt \tag{1}$$

The Failure Rate (FR), which is also denoted as $\lambda(t)$, function is defined as the ratio of the PDF and the $R(t)$:

$$\lambda(t) = \frac{f(t)}{R(t)} \tag{2}$$

Such approach, allows to bring down the abstract concept of the Reliability or the Reliability Modelling to the simple fitting a proper mathematical distribution to the observed data. Such mathematical distributions, which are commonly used in reliability engineering, are often called a Lifetime Distributions (LD), and they are listed below [109]:

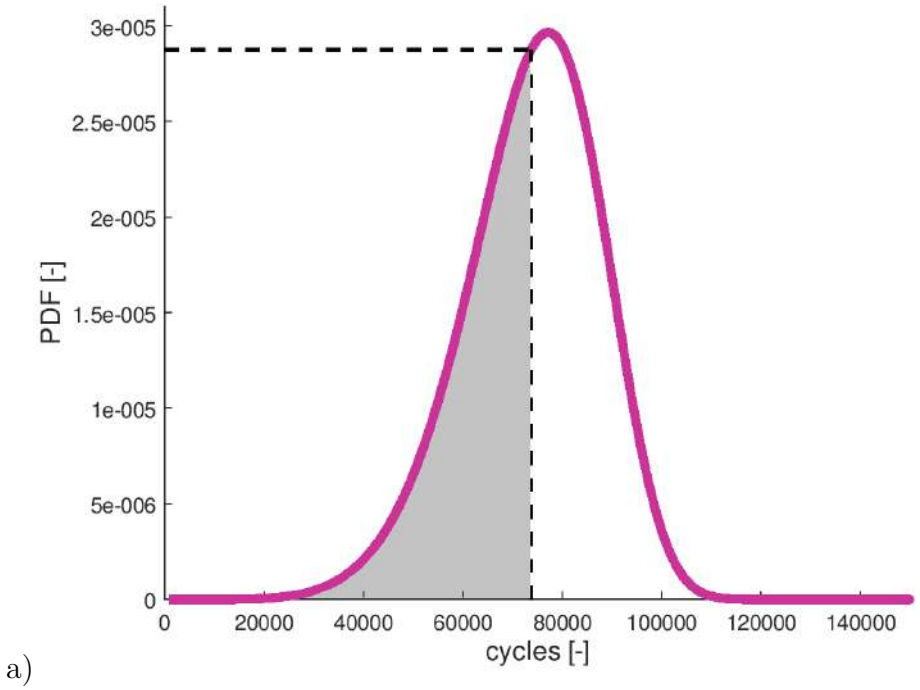
- the Exponential Distribution,
- the 2- or 3- parameter Weibull Distribution,
- the Multimodal Weibull Distribution,
- the Normal Distribution,
- the Lognormal Distribution,
- the Gamma Distribution,
- the Logistic Distribution,
- the Loglogistic Distribution,
- the Gumbel Distribution.

However, in practical discussions over reliability of either single components, modules or whole systems, the Bathtub Curve concept is used far more often than complex LD analysis. The Bathtub Curve is a simplified, graphical representation how the $\lambda(t)$ changes over time. As depicted in Fig. 14 it can be divided into three regions:

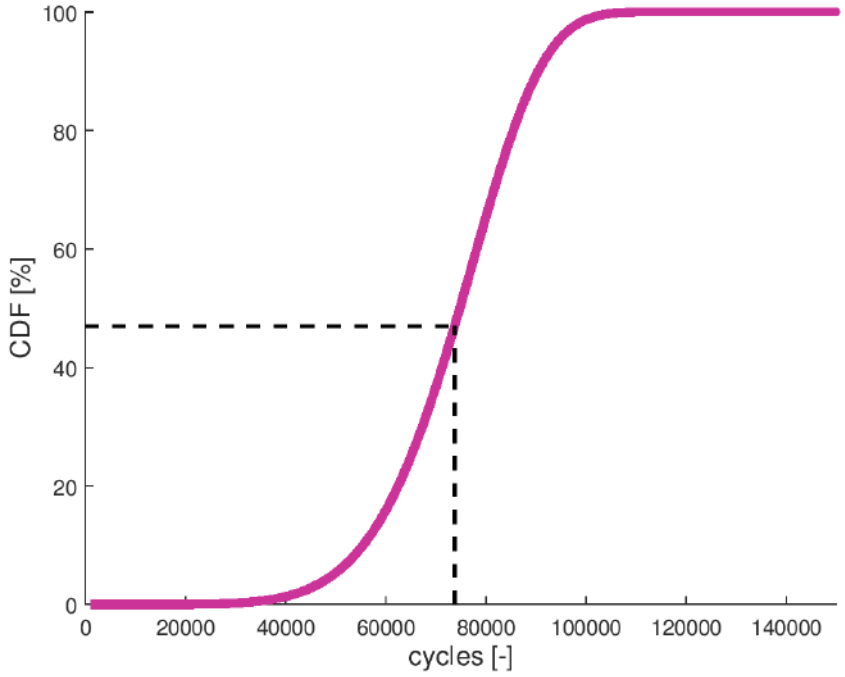
1. the *Infant Mortality* or *Intrinsic Failure* region, where failures are mostly caused by internal defects or impurities, and they are strictly related to the quality of the manufacturing process,

2. the *Useful Lifetime* or *Random Failure* region, where failure rate is relatively constant, and failures are the result of a strictly random phenomena,

3. the *Fatigue Failure* or *Extrinsic Failure* region, where probability of failure significantly increases due to progressing wear-out of the device.



a)



b)

Figure 13. Examples of Probability Density Function (PDF) a), and Cumulative Density Function (CDF) b) of the Weibull model depicting fatigue mechanism of solder joint, in dependence of number of thermal cycles performed by this joint. The corresponding value of surface beneath PDF curve was marked on the CDF plot.

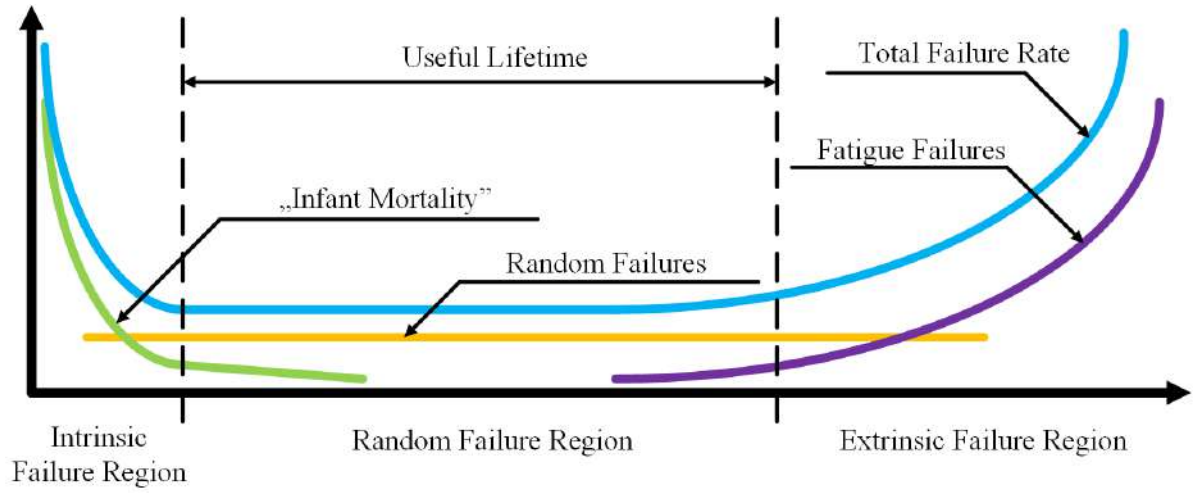


Figure 14. The Bathtub Curve used for graphical representation of failure rate changes over time [110].

In general, quality issues - e.g. the famous self-ignition of lithium-ion batteries in smartphones [111] - are not in the scope of the reliability engineering, and it is expected that all *Infant Mortality* failures are properly screened out from general population thanks to extensive in-house testing and thorough quality gates. Thus, the Bathtub Curve concept allows to simplify reliability modelling to two questions:

1. „How high will be the Failure Rate?" and,

2. „How long the Failure Rate will remain constant?".

Thanks to the assumption that the FR shall be relatively constant for certain period, it is possible to use the Exponential Distribution for the reliability modeling. As presented in the next paragraph, this greatly simplifies calculations required for reliability assessment. The second question in fact defines so-called the Useful Lifetime (UL) - the time of operation in certain conditions, after which device should be replaced. Although other definitions of useful lifetime are also possible, the most common approach is to assume that End of Life (EoL) is when degradation initiates, and therefore the wear-out failures may occur.

Typically, the Failure Rate ($\lambda(t)$) is denoted in Failures In Time (FIT) - the amount of failures per 1 billion (10^9) hours of operation. This approach is very common across

manufacturers of power electronics components, thanks to its simplicity - the target $\lambda(t)$ calculation is brought to a simple multiplication of Base Failure Rate (λ_0) and proper correction factors, each for different stressor. A great example of such approach is a $\lambda(t)$ estimation for foil or ceramic capacitors [112, 113], for which both Blocking Voltage Correction Factor (π_V) and Operating Temperature Correction Factor (π_T) have to be taken into account, as presented in Eq. (3). Practical example of such calculations is presented in Section 4.1.

$$\lambda = \lambda_0 \cdot \pi_T \cdot \pi_V \tag{3}$$

Other parameters, which are often used to quantify reliability of repairable and non-repairable devices during their UL are the Mean Time Between Failures (MTBF) and the Mean Time To Failure (MTTF). Both MTBF and MTTF are usually denoted in hours (h) or years (y). Moreover, thanks to properties of the Exponential Distribution, MTBF or MTTF can be easily converted into the $\lambda(t)$, with Eq. (4):

$$\lambda = \frac{1}{MTBF} \tag{4}$$

The alternate, and yet very popular approach is estimation of the Annual Failure Rate (AFR). However, there are no single definition of the AFR, and this acronym is also used for the Annualized Failure Rate or Average Failure Rate, thus various manufacturers may use different strategy to calculate its value [114]. Examples of various formulas used for AFR estimation are presented in Eqs. (5) - (12).

$$AFR_1 = \frac{Total\ number\ of\ failures\ in\ time\ interval\ (T1 - T2)}{Total\ cumulative\ working\ time\ in\ interval\ (T1 - T2)} \tag{5}$$

$$AFR_2 = \frac{Total\ number\ of\ failures\ in\ 1\ year}{Total\ working\ time\ accumulated\ in\ 1\ year} \tag{6}$$

$$AFR_3 = \frac{Total\ number\ of\ failures\ in\ last\ 12\ moths}{Total\ installed\ base\ of\ devices} \tag{7}$$

$$AFR_4 = \frac{Number\ of\ failures\ in\ 12\ consecutive\ months}{Cumulative\ installed\ base\ at\ the\ end\ of\ the\ same\ 12\ months} \tag{8}$$

$$AFR_5 = 100 \cdot \frac{12}{m} \cdot \frac{Number\ of\ failures\ in\ m\ consecutive\ months}{Cumulative\ installed\ base\ at\ the\ end\ of\ the\ same\ m\ months} \tag{9}$$

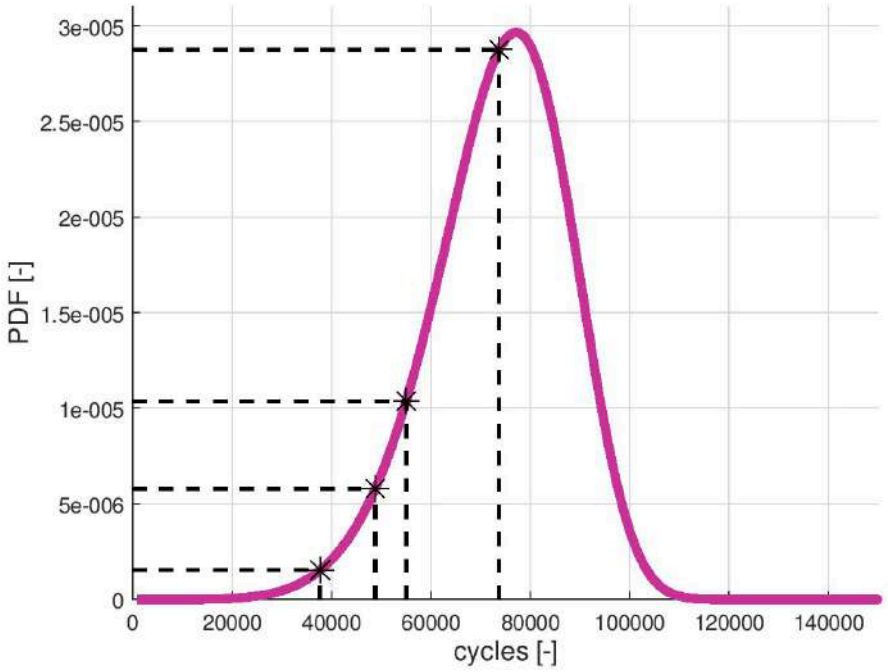
$$AFR_6 = E_f \cdot \frac{Total\ number\ of\ failures\ in\ m\ months}{Total\ working\ time\ accumulated\ in\ m\ months} \tag{10}$$

$$AFR_7 = \frac{8766}{MTBF} \tag{11}$$

$$AFR_8 = 1 - e^{\frac{-8766}{MTBF}} \tag{12}$$

In contrast to the Failure Rate ($\lambda(t)$), the UL may be expressed in time units (e.g. hours or years), as well as amount of cycles (e.g. thermal, mechanical or read-write), depending on the physics of the dominant degradation mechanism. Similar to the AFR, various manufacturers have different approach for identification of the UL. As an example, for IGBT modules, Infineon defines the useful lifetime based on the ALT results, as a time until 5% of population will reach the EoL criteria, indicating degradation of the device. In contrast to the IGBT modules, Infineon uses the 1%, 5% or 10% threshold for discrete devices [115]. Other common approach is to use the mean value of the LD, identified based on the ALT results. The graphical comparison between these criteria are depicted in Fig. 15, where the PDF and corresponding the CDF for example ALT results are given. As presented, the UL is heavily dependant on the approach or the strategy used for calculations. This discussion shows the one of most challenging obstacles related to the DfR methodology - lack of the well-standardized, easy-accessible reliability data.

As it was mentioned earlier, the DfR is based on the idea that overall reliability of any power converter, or power electronic functional module, can be estimated for a pre-defined set of stressors, based on known reliability models of critical components used in this converter or module. Moreover, analysis of the Bathtub Curve indicates, that failure modes for each critical component can be divided into three groups: the Intrinsic Failures, the Random Failures and the Extrinsic or the Wear-out Failures. Thus, the second foundation of the DfR is a vast knowledge about critical components, failure modes and degradation mechanisms typical for these critical components and their reliability models. Closer analysis of a cross-comparison of typical failure modes, stress functions and reliability models for power semiconductor devices, presented in Fig. 1, reveals the next challenge related with the practical implementation of the DfR into engineering



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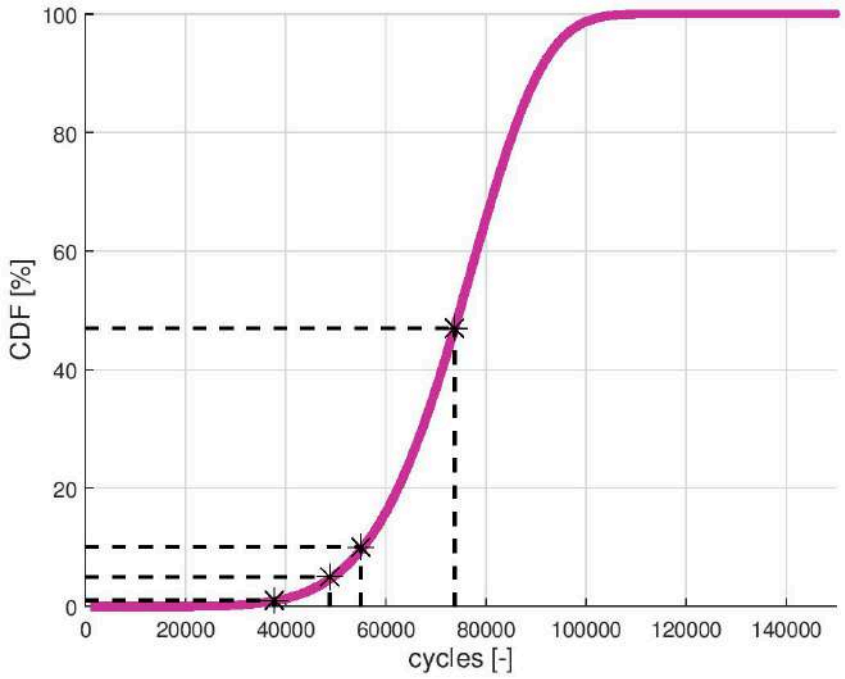


b)

Figure 15. The Probability Density Function (PDF) a), and the Cumulative Density Function (CDF) of the example Weibull distribution, depicting probability of failure of solder joint in dependence of number of thermal cycles performed by this joint. 1%, 5%, 10% and mean value of distribution are marked with dashed black lines.

workflow - multiplicity of reliability models. This aspect is especially challenging, as there are numerous types of critical components in the HPPS, such as:

- power semiconductor devices,
- integrated circuits (e.g. FLASH memory, operational amplifier, analog-to-digital converter, etc.)
- capacitors,
- magnetic components (e.g. chokes, inductors and transformers),
- solder joints,
- relays and breakers,
- mechanical components (e.g. connectors, terminals),
- and many others.

And for each type of critical component, a list of stressors, failure mechanisms and reliability models, similar to the example given in Tab. 1, can be prepared. Repetitive Short Circuit Conditions (RSCC) and how they affect on degradation mechanisms in power MOSFETs are discussed in [116, 117].

Table 1. Failure modes and degradation mechanisms suitable for power MOSFETs.

Type	Failure Mode	Stressors	Ref.
Intrisic	Stacking Fault (SF)	RSCC I_{DS}	[118, 119]
	Hot Carrier Injection (HCI)	V_{GS} V_{DS} T_J	[120]
	Time-Dependent Dielectric Breakdown (TDDB)	V_{GS} V_{DS} T_J	[121, 122]
Random	Self turn-on, Activation of parasitic BJT	du/dt, T_J	[123]
	Single Event Effects (SEE)	V_{DS}, T_J	[124]
	TDDB	V_{GS}	[121, 122]
Extrinsic	Electromigration	I_{DS}, T_J	[125]
	Solder joint fatigue	I_{DS}, T_J, ΔT_J	[126]
	Bond wire lift-off	I_{DS}, T_J, ΔT_J	[127]
	Bond wire heel-cracking	I_{DS}, T_J, ΔT_J	[128]
	Solder delamination	T_J, ΔT_J	[129, 130]
	Brittle cracking	T_J, ΔT_J	[131]
	Aluminum reconstruction	I_{DS}, T_J	[132]
	HCI	V_{GS} V_{DS} T_J	[120, 133]
	TDDB	V_{GS} V_{DS} T_J	[134, 135]
	Avalanche Gate Breakdown (AGB)	V_{DS}	[121, 133]
	Corrosion	V_{GS} V_{DS} T_J	[136]
	Thermal runaway	RSCC	[137, 138]

The reliability model parameters, which are defined for each failure mode separately, are unique for each component, as they depend on the structure (e.g. thickness and length of wire bonds) and manufacturing process (e.g. cooling ramp) of the critical component itself. Thus, the reliability model prepared for one component, e.g. power MOSFET from manufacturer A, may not be adequate for counterpart from manufacturer B. In practice, it means that to prepare reliability model for each new component, multiple ALTs have to be prepared, for each failure or degradation mode separately, which makes reliability engineering very cost extensive research. This aspects is further discussed in chapter 3. Unfortunately, such detailed data as PDFs, ALT reports or reliability models are rarely provided by manufacturers.

2.3 Modified Design for Reliability (DfR) procedure for short lifespan projects

Typically, the DfR procedure consists of the following steps [139, 140]:

1. mission profile and environmental parameters definition,
2. system-level mission profile evaluation,
3. circuit modelling,
4. stressors levels evaluation for critical components,
5. reliability evaluation for critical components,
6. system-level reliability assessment.

As it is presented in Fig. 16, there are two approaches for DfR: either chosen topology is released for design phase after successful reliability assessment [139] or designed functional module is released for production after successful reliability assessment [140]. Unfortunately, both procedures are extremely time-consuming, as they base on complex simulation studies and electro-thermal modeling. Thus, the classical DfR concept may not be suitable for projects with a short lifespan or Time To Market (TTM). As an example, a typical TTM of moderate complexity project in the automotive industry is between 40 and 70 months [141], while in some highly specialized applications (e.g. plasma processing industry) first functional prototype has to be delivered within $6 - 15$ months from agreement on technical specification. For such specialized applications a modified DfR procedure (see Fig. 17) was proposed, which consists of the following steps:

1. boundary condition definition,
2. simulation stage,
3. design stage and initial reliability evaluation,
4. Proof of Concept (PoC) laboratory testing,

5. Reliability Growth,

6. Reliability Demonstration,

7. Reliability Maintenance.

The main difference between the classical and the proposed approaches is a higher integration of DfR procedure with the engineering workflow, allowing to get either Proof of Concept (PoC) or fully functional prototype available sooner. Thus, the modified procedure is rather focused on the laboratory testing, than on the extended electro-thermal simulation study.

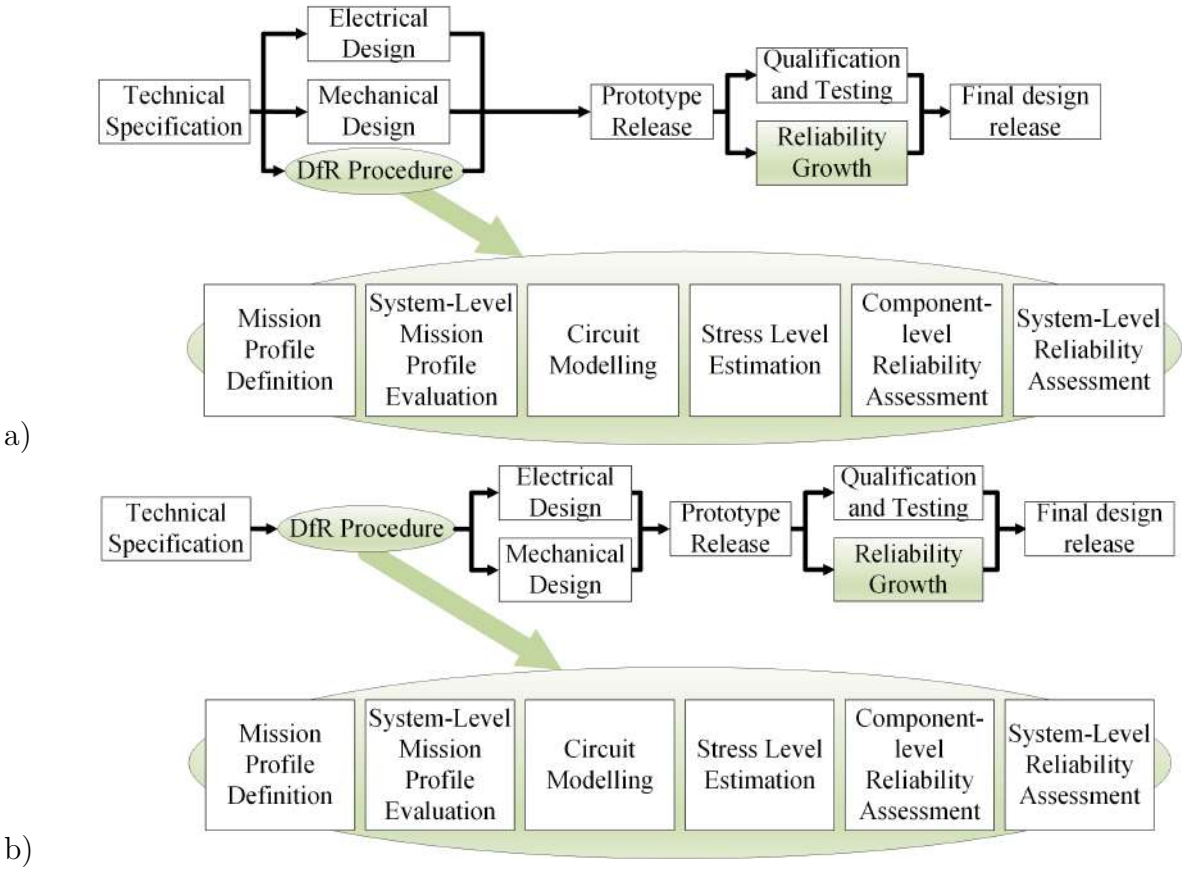


Figure 16. The typical Design for Reliability (DfR) procedure presented in respect to the design process workflow, if the DfR procedure is performed before electrical and mechanical design a), if the DfR procedure is performed in parallel to electrical design b). Steps of the typical DfR procedure and reliability growth are marked with green color [110].

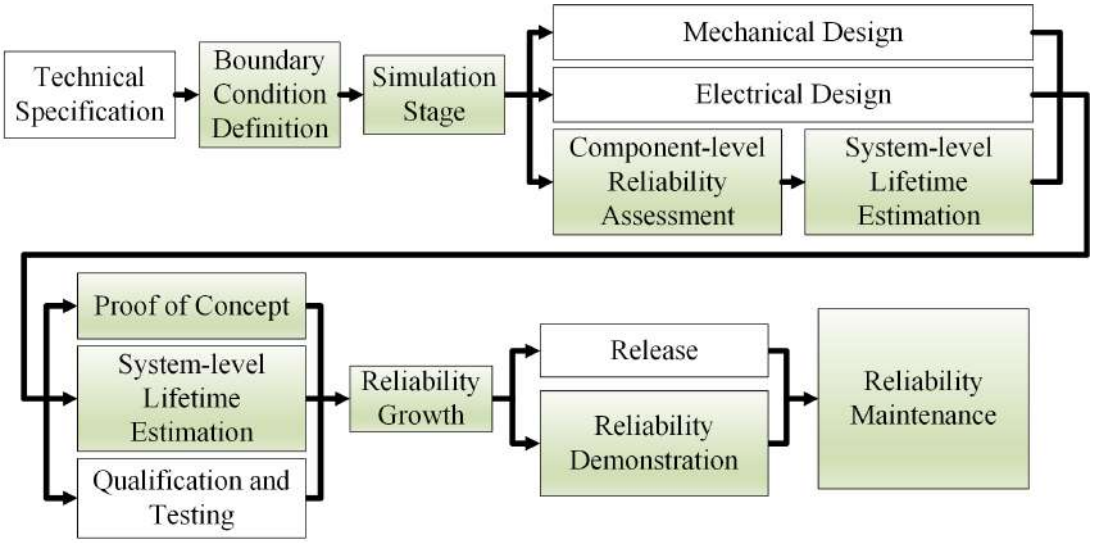


Figure 17. The modified Design for Reliability (DfR) (green blocks) procedure presented in respect to the design process workflow [110].

The first stage of both the modified and the classical DfR procedure is similar - boundary conditions have to be defined. In this step, the system designer has to define not only the expected mission profile or environmental parameters (e.g. humidity, altitude, ambient temperature, presence of technical gases) but also the functional requirements of a power converter, desired efficiency, desired overall cost, or reliability goals. This step is the very foundation of the whole designing process as operating conditions define stress levels (e.g. humidity), which directly affects on the corresponding degradation mechanisms (e.g. corrosion [136]).

The next step is the simulation study. In the classical approach, the goal of the circuit modeling and the comprehensive electrothermal simulations is the accurate estimation of stress levels, like maximum junction temperature swing per cycle. In contrast, the main goal of the simulation study in the proposed DfR procedure is the selection of the most promising topology, which allows for compliance with all functional requirements (e.g. minimum efficiency, ripples, etc.). Secondary goals of the simulation stage are the selection of passive and active components (e.g. capacitors, power semiconductors) and the rough stress level estimation. At this step, reliability evaluation is focused rather on verification if all critical components operate within Safe Operating Area (SOA)

than MTBF calculation. Thus, if electrical or electro-thermal model are not available, simulation study can be performed based on the ideal components. Then, concept of analysed module or power converter is released for the electrical and mechanical design.

In the proposed DfR methodology, the first reliability assessment is performed simultaneously to the design process of a very first prototype of the power converter. For this purpose, stress levels can be taken either from the rough estimation performed in the previous step, or they can be assessed based on proper electrical and electro-thermal simulations which include assumed mission profile or worst-case operating conditions [107]. Then, simulation results are applied to reliability models of each critical component to estimate its UL. At last, the overall reliability of the designed circuit can be estimated as superimpose of particular components reliability, based on the Reliability Block Diagram (RBD) [142], the Markov Diagram (MD) [143], the Fault-Tree Analysis (FTA) [144] or other assessment method. The paralleling of the reliability assessment and design procedures (e.g. mechanical design, electrical schematic preparation, PCB routing, etc.) allows for significant time-saving and reduces risks related to the inaccuracy of any electrical- or electro-thermal simulation study. As an example, if stress levels would be significantly underestimated due to insufficient model accuracy, the sooner the prototype will be manufactured, the sooner this issue will come up and the higher chances are that problem will not affect on assumed delivery date. Moreover, if the reliability assessment suggests that reliability goals, defined at the very first stage of discussed modified DfR procedure, may not be fulfilled, it is possible to adjust the design properly or propose countermeasures.

The main purpose of the PoC, the first prototype of the newly developed power converter, is qualification testing of chosen topology, to verify if all functional requirements are fulfilled and to detect most of the design flaws. For this purpose, all key signals and stressors (e.g. voltage and current waveforms, temperatures) are measured and compared with simulation results. If measured stress levels are similar to values estimated during the simulation stage, it is expected that reliability goals will be fulfilled. If there would be a discrepancy between real-life measurements and estimated values, proper adjustment

of MTBF calculations should be performed, to verify if reliability goals are still met. In practice, measurement of certain stressors may be quite tricky, due to very limited access to critical component, as an example:

- junction temperature of encapsulated power semiconductor devices,
- working current of each semiconductor device in a multichip module,
- ripple current of capacitor bank,
- etc.

Unfortunately, such measurements may require heavy interference into the tested circuit, which may affect on the performance of tested power supply or measurement accuracy.

The next step in this process is the iterative improvement of developed power supply, called also the Reliability Growth. This stage covers a wide span of test procedures designed to push power converter to limits and mark its weakest links. Typical tests defined for this step are e.g. the Multi-Stressor Test (MST), the Overload Test, the Highly-Accelerated Life Test (HALT), the Highly-Accelerated Stress Test (HAST), the Step Stress Test (SST). Each detected malfunction is immediately analyzed to determine and remove the root cause - only then the test procedure is restored. Thus, this step ends with a verified, well-tested, and bug-free final design.

The last stage of the DfR procedure is the Reliability Demonstration of a final product, to verify if assumed reliability goals are truly fulfilled. It is confirmed based on proper ALT, which not only introduces high-stress conditions for all critical components in the tested module or HPPS but also - mimics target operating conditions. Afterwards, the final product is released for a mass production and stops being the object of interest of Research and Development department.

Although the DfR procedure ends with the Reliability Demonstration from the product development point of view, it is only the beginning of HPPS lifecycle, during which many challenges have to be overcome. To address these challenges, the additional step of DfR procedure is proposed - the Reliability Maintenance, which focus on ensuring that reliability goals will be fulfilled for all manufactured units, independently to the

production batch, or time and place of assembly. Thus, this step partially overlaps with the Quality Control concept. The very fundamentals of the Reliability Maintenance are:

- definition of Quality Gates or Start-Up procedures, which ensure that field reliability of HPPS will not be compromised by Infant Mortality failures,
- monitoring of field reliability data (e.g. $\lambda(t)$, AFR) and customer feedback, in order to confirm if reliability goals are fulfilled,
- if necessary, preparation of the On-going Reliability Test (ORT) - the ALT of HPPS from different batches or production lines, in order to confirm that reliability goals are fulfilled for mass produced HPPS,
- component obsolescence management and obsoletes counterparts qualification, to ensure that any change in design will not negatively affect reliability of the HPPS.

Reliability Maintenance is also a key difference between modified and traditional DfR procedure.

2.4 Conclusions

Discussion presented in this chapter shows that DfR is the most suitable approach for reliability improvement of HPPSs for plasma processing. Moreover, mathematical apparatus presented in this paper allows to precisely define reliability criteria for HPPSs, which is essential for reliability-oriented design. At last, definition and critical evaluation of DfR procedure shows that traditional approach is not suitable for short lifespan or short Time To Market (TTM) projects. To address these challenges, a modified DfR procedure was proposed.

Next, analysis presented in this chapter allows to distinguish main challenges related to the practical side of the reliability-oriented design:

- lack of standardization of the reliability data provided by manufacturers - if any reliability data are given,
- lack of easy-accessible reliability models or reliability data for critical components, which could be further used in component-level or system-level reliability assessment of modern HPPS,

- lack of easy-accessible electrical or electro-thermal models of semiconductor devices, which could be further used in simulation study of modern HPPSs,
- accuracy and reproducibility of measurement techniques, used for stress level estimation for critical components operating in fully assembled power supply, which is essential for laboratory testing of PoC and further versions of newly developed HPPS,
- lack of industry-friendly, simplified test procedures for reliability-oriented comparative testing, for purposes of the Reliability Maintenance.

These technical challenges have to be overcome in order to successfully implement proposed DfR procedure into any engineering workflow. Thus, following tasks and work packages can be identified:

1. Development of reliability models for each critical component used in the modern HPPS.

2. Development of industry-friendly, cost-efficient approach for preparation of the reliability model for each critical component used in the modern HPPS.

3. Development of industry-friendly, cost-efficient approach for preparation of electrical or electro-thermal models of semiconductor devices used in modern HPPSs.

4. Development of dedicated tools and measurement procedures, to ensure that during laboratory testing of HPPS, key stressors are estimated with sufficient accuracy, repeatability and reproducibility for each critical component.

5. Development of industry-friendly, cost-efficient methods for simplified accelerated lifetime testing, for purpose of reliability-oriented comparative study of counterparts of critical components used in the modern HPPS.

However, all of these work packages can not be covered in single PhD thesis. Thus, further analysis was required to define priorities on them. Statistical studies suggests that over 21% failures of power electronic systems for renewable energy is related to the power semiconductor devices [145]. Although there was no similar survey among manufacturers

of power converters for plasma processing applications, it is expected that the power semiconductor devices are the root-cause of over 41.2% of HPPS failures. Therefore, actions focused on this type of critical component shall have the highest impact on the overall reliability improvement of the modern HPPSs.

Whus, to address these challenges, a research over development of the reliability model for SiC power MOSFET in $SOT-227B$ housing was initiated. Investigation presented in this thesis focuses not only on the identification of the reliability model parameters, but also answers the question how to do it in industry-friendly, cost-efficient manner. Such reliability model can be further used for the reliability evaluation in proposed DfR procedure, by means of e.g.:

- Useful Lifetime (UL) estimation,
- Failure Rate ($\lambda(t)$) estimation,
- Mean Time Between Failures (MTBF) or Mean Time To Failure (MTTF) estimation.

The detailed description of this study is presented in the next chapter.

Chapter 3

Reliability modelling of SiC power MOSFET

As presented in chapter 2, encapsulated SiC power MOSFETs are subjected to multiple failure or degradation mechanism, but not all of them are really in the scope of the reliability-oriented design strategy. The *Infant Mortality* failure modes are strictly related to the quality of the manufacturing process, and they are excluded from the scope of DfR. Thus, only *Random* and *Extrinsic* failure modes shall be modelled with proper LD. However, identification of the reliability model parameters for each degradation mechanism, according to the Physics of Failure (PoF) concept, requires preparation of multiple ALTs, each optimized for different failure mode, which is very expensive and time consuming. To overcome this challenge, chosen failure modes (solder delamination, solder joint fatigue, bond wire lift-off, bond wire heel-cracking, brittle cracking) might be considered as single *fatigue-like* failure mode. This approach is much more suitable for some industrial customers of power electronics (e.g. power converter manufacturers) than the typical PoF, as it is easier to implement and more cost effective. Moreover, the examination of power semiconductor device which have failed in the field, often does not allow to determine which particular degradation mechanism led to failure. In this chapter, the procedure of identification of reliability model parameters for such *fatigue-like* failures of encapsulated SiC power MOSFETs, is presented. Discussion covers all technical aspects of reliability modelling, starting from the analysis of Accelerated Lifetime

Testing strategies, through designing the dedicated test bench, up to identification of the mathematical model parameters.

3.1 Accelerated Lifetime Test Methodology

The fundamental rule of the ALT is to design a test in such a way, to accelerate only desired failure mechanism - in this case a *fatigue-like* failure modes. Typically, researchers have used the Thermal Cycling (TC) and the Power Cycling (PC) for this purpose [146, 147], referred also as *passive* and *active* cycling respectively. These studies have shown that several challenges in the PC have to be resolved in order to obtain reliable and accurate test results, which would be suitable for the lifetime estimation of power semiconductor devices. These challenges may be divided into two groups: methodical and technical. Moreover, methodical differences between test strategies heavily limits possibilities to compare test results [148].

3.1.1 Thermal, Power and Current Cycling

The very foundation of the TC concept, is to keep temperature swing constant over the test progress, to investigate the physical basics of fatigue failures - the crack expansion rate, progress of the delamination or the grain growth in the solder joint [149, 150]. The main idea behind such approach is to monitor a pre-defined electrical, physical or chemical parameters, also called health indicators, in order to make an indirect SoH estimation of the tested device. Furthermore, such test results may be used to implement the physical laws of the fatigue into e.g. Finite Element Method models and to adjust those models to reality [151].

The alternate approach is the PC test, during which the power level is kept constant during test instead of temperature swing. As Device Under Test (DUT) degrades, the thermal impedance increases, causing higher peak junction temperature during pulse time, which additionally accelerates the degradation mechanism. Therefore, when the test is performed without this self-acceleration mechanism, the lifetime of the power module is approximately three times longer, as presented in [146, 152].

Such a large difference is caused by a significant distinction in the PoF induced during the TC and the PC. In case of the TC, due to the technical limitations of thermal chambers, the temperature slope is quite low - it varies from 50 $\frac{^{\circ}C}{min}$ to 70 $\frac{^{\circ}C}{min}$. In contrast, the temperature slope during power cycles is limited only by the thermal capacitance of the heatsink used for the cooling of DUTs. Therefore, the mechanical stress in the tested structure, induced by differences in the thermal expansion coefficients between SiC structure, solder joint and bond wire, is much higher in the case of PC test [153]. Moreover, there is no current flowing through the DUT during the TC, thus bond wires are not subjected neither to any excessive heating, nor any Lorentz force, which cause additional mechanical load to bond wires [154].

Although, recent study [155, 156] does not distinguish difference between the PC and the Current Cycling (CC), they shall not be treated as same concept. In the CC test, the heating current is kept constant during the test, instead of the power dissipated across DUTs. Thus, power dissipation also increases along the test duration, accordingly to progressing degradation of semiconductor device. Simply, increased On-state Channel Resistance ($R_{DS_{ON}}$) or On-state Collector-Emitter Voltage Drop (V_{CE}), results in higher power dissipation for the same current conducted through tested device, which ends up in higher Peak Junction Temperature ($T_{J_{MAX}}$) and Amplitude of Junction Temperature Swing (ΔT_J) per cycle. In fact, this is the next self-acceleration mechanism, which may additionally shorten UL of power semiconductor devices.

Similarly to the comparison of the TC and the PC test results, research presented in [146] indicates that there is significant difference between the PC and the CC test results. The self-acceleration mechanism described in previous paragraph, makes degraded semiconductor device to fail far faster, if it is subjected to the CC test than in the case of the PC test. However, such self-acceleration mechanism should not be present at all, until the degradation of semiconductor device initiates. Author states, that the PC and the CC shall be considered as equivalent if the EoL criteria, is the initiation of semiconductor device degradation. If the EoL criteria chosen for the ALT is the fatal failure, than the

control strategy which better corresponds to the real-life operating conditions should be chosen. EoL criteria are broader discussed in further parts of this dissertation.

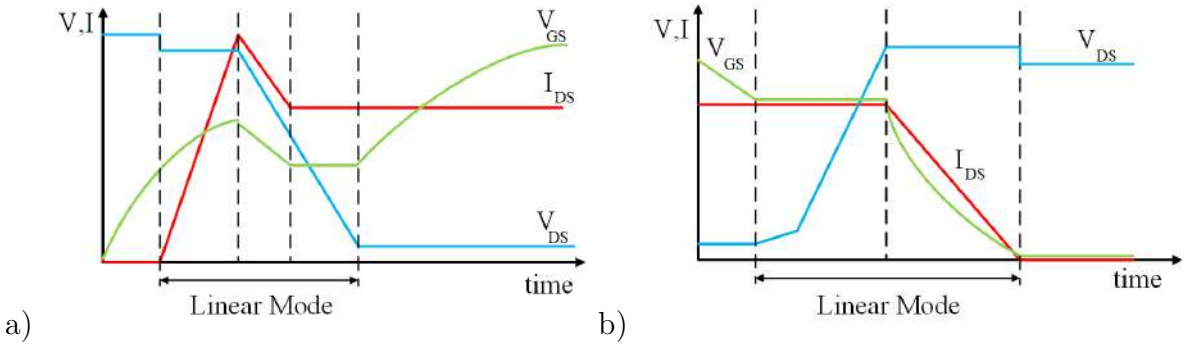


Figure 18. Voltage and current during a power MOSFET switching conditions.

Summarizing the discussion, the PC and the CC tests are far better representation of the real-life applications than the TC. In a typical power electronic converter, there will be no compensation of the self-acceleration mechanism of power semiconductors degradation rate - a power supply works with a specific load and has to deliver the desired amount of power to it, without consideration about the operating conditions the power electronic components within. Moreover, in the real application not only does the MOSFET itself degrade, but also the thermal interface between it and the heatsink. This phenomena additionally increases the junction temperature swing for the same level of dissipated power. It is certain, that the CC test offers the best projection of operating conditions, where conduction losses dominates - as in the case of railway or grid applications. However, thanks to their superior performance (e.g. low gate charge and parasitic capacitance), in modern HPPS *SiC* power MOSFETs are typically used in high-frequency hard- and soft-switching applications, where switching losses dominates. Unfortunately, switching losses are not only dependant to the SoH of the power semiconductor device, but also on various exterior and environmental conditions - e.g. driver circuit, ambient temperature, load, etc. Moreover, during switching conditions power MOSFET is subjected to the linear mode operation, as it is depicted in Fig. 18. Thus, for very high switching frequencies, the linear mode operation may take significant part of the time, or even dominate over operation in saturation region. As the main goal

of the ALT is the best possible projection of real-life operating condition, this aspect also has to be taken into account. In the case of the PC test, it is possible to keep the DUT in the ohmic region of the output characteristic during whole duration of the ALT, by simple adjustment of power MOSFET's Gate-Source Voltage (V_{GS}). In contrast, in the typical CC test power MOSFETs are kept fully saturated. Thus, for the ALT of power semiconductor devices used in the state-of-the-art HPPS for plasma processing, the PC test is found more suitable than the CC test.

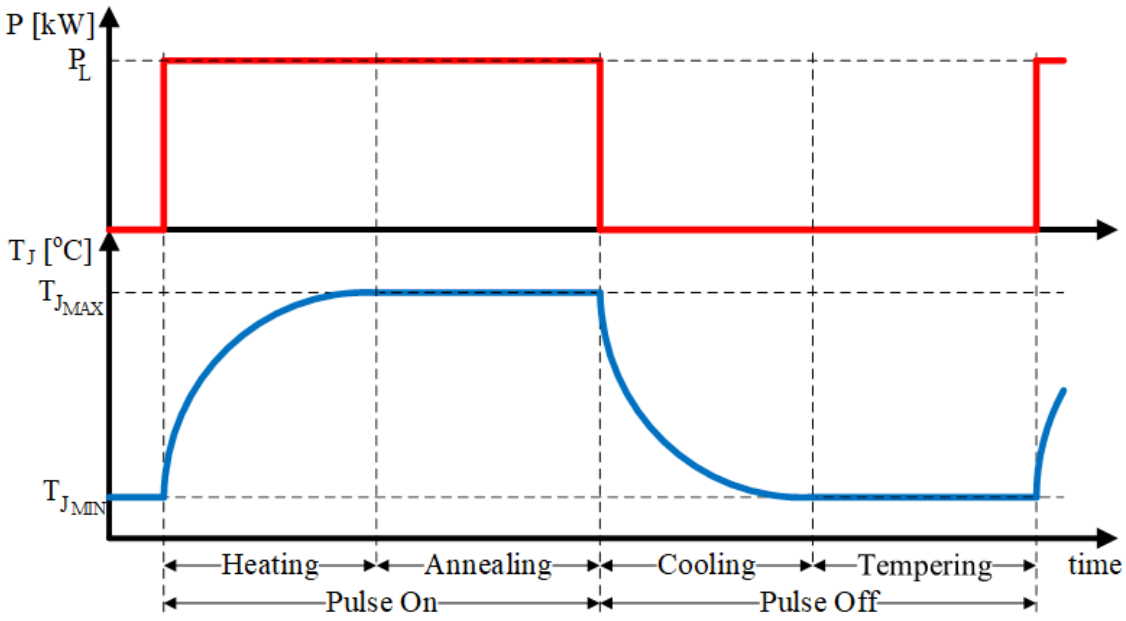


Figure 19. Typical heating cycle for the Accelerated Lifetime Test (ALT) procedure with distinguished particular cycle steps.

The last methodical issue, common for all types of ALTs, is to determine a proper heating phase, also called the Pulse On-time t_{ON}, and cooling phase duration, referred also as Pulse Off-time t_{OFF}. An example of a power and temperature envelope during a single cycle is shown in Fig. 19. A typical approach is to decrease the annealing and tempering time (also called "dwell time") to shorten the overall cycle period and, as a result, shorten the whole test duration. Unfortunately, the mechanical tensions present inside the tested power semiconductor slowly relaxes during the dwell time. In such a case, an excessive reduction of dwell time may result in shortening the lifetime of the tested sample, through extended impact of the mechanical tensions on the semiconductor

structure [157]. As a result, thermal cycles or mild-slope power cycles with long dwell-time are preferable for e.g. solder delamination and grain growth, unlike short power cycles, which mostly introduce bonding-related failure modes. These facts stress the importance of testing power semiconductors in conditions close to the real application.

3.1.2 The End of Life (EoL) Criteria

The next fundamental decision, with a significant impact on both the design of the ALT and the test results, is chosen EoL criteria, which may be either significant degradation of DUT or fatal failure. In the first case, typical health indicators are: Gate-Source Leakage Current ($I_{GS_{LKG}}$), Drain-Source Leakage Current ($I_{DS_{LKG}}$), Gate-Source Threshold Voltage ($V_{GS_{TH}}$), On-state Channel Resistance ($R_{DS_{ON}}$), Body Diode Forward Voltage Drop (V_{FWD}) and Junction-to-Case Thermal Impedance ($Z_{TH_{JC}}$). Significant drift of these parameters from their nominal values, as listed in Tab. 2, indicates heavy degradation of the DUT. All of these parameters are useful; however, none of them is universal as each of listed health indicators is related to a different degradation mechanism. Thus, a proper health indicator should be defined during the design phase of ALT, and it should be suitable for the failure mode under the examination.

Table 2. End of Life (EoL) criteria for *SiC* power MOSFETs [155, 158]

Parameter	$I_{GS_{LKG}}$	$I_{DS_{LKG}}$	$V_{GS_{TH}}$	$Z_{TH_{JC}}$	$R_{DS_{ON}}$	V_{FWD}
Threshold	+100%	+100%	±20%	+20%	+2%	+2%

As presented in [159], $I_{GS_{LKG}}$ and $I_{DS_{LKG}}$ may not change at all in the lifespan of the tested semiconductor, while there are significant changes in either $R_{DS_{ON}}$ or V_{FWD}. On the other hand, multiple studies [103, 160] have shown that both $I_{GS_{LKG}}$ and $I_{DS_{LKG}}$ spikes just before the fatal failure of power MOSFET. Both of these indicators are strictly related to the state of the semiconductor chip itself, as the $I_{GS_{LKG}}$ increases sharply when the gate oxide fails. Similarly, $I_{DS_{LKG}}$ spikes after the failure of a single MOSFET cell inside the chip. Another health indicator, which describes the state of the gate oxide is the $V_{GS_{TH}}$. In contrast to $I_{GS_{LKG}}$, this parameter changes slowly over the lifespan of the power MOSFET, according to the gate oxide degradation progress.

A well-known health indicator used in either the PC or the CC testing of power modules is $Z_{TH_{JC}}$. This parameter changes as solder between either semiconductor chip and paddle or paddle and baseplate delaminates, due to degradation of the soldering between them [161]. Thus, it is mostly used to monitor solder delamination progress.

The electrical parameters commonly used for evaluation of aging of bond wires are $R_{DS_{ON}}$ and V_{FWD} [162]. These two indicators seem to be equivalent, but such hypothesis might be misleading. As presented in Fig. 20, $R_{DS_{ON}}$ measured at the terminals of encapsulated power MOSFET consists of components like: Solder Resistance (R_S), Bond Wire Resistance (R_B), drain and source Terminal Resistance (R_T), Channel Resistance (R_{Ch}), Accumulation Region Resistance (R_A), JFET Region Resistance (R_{JFET}), Drift Region Resistance (R_D) and $N+$ Region Resistance (R_{Subs}) [159]. As MOSFET's R_{Ch} is dependent on $V_{GS_{TH}}$, and R_A is dependent on Flat-band Voltage (V_{FB}), $R_{DS_{ON}}$ increases according to the degradation of the gate oxide, as both threshold voltage and accumulation region resistance suffer degradation due to the drift in the interface charge. In contrast, V_{FWD} measured at the source-drain terminals is not $V_{GS_{TH}}$ dependent, but still contains information about interconnection resistance. Because of this, it should remain constant throughout all PC test, until the bond wire fails.

Usage of typical EoL criteria (see Tab. 2) allows to significantly shorten the duration of the ALT, but has a significant drawback - it does not provide any information about *how long* the damaged sample will work before a fatal failure. This is not critical in the case of ALTs designed for scientific purposes, like investigation of the physical basis of fatigue failures; nevertheless, it becomes significant in the case of building an empirical reliability model for commercial purposes. Therefore, in presented study following approach was chosen: the EoL criteria for tested *SiC* power MOSFETs was fatal failure, but for monitoring of the degradation process two health indicators were recorded: $R_{DS_{ON}}$ and V_{FWD}. As presented in previous paragraph, these parameters are excellent for the bond wire degradation monitoring, which is in scope of *fatigue-like* failure mode definition, and for which the presented PC test is optimized for. Other strategies for degradation monitoring which are worth mentioning are $T_{J_{MAX}}$ measurement, and V_{DS} measurement.

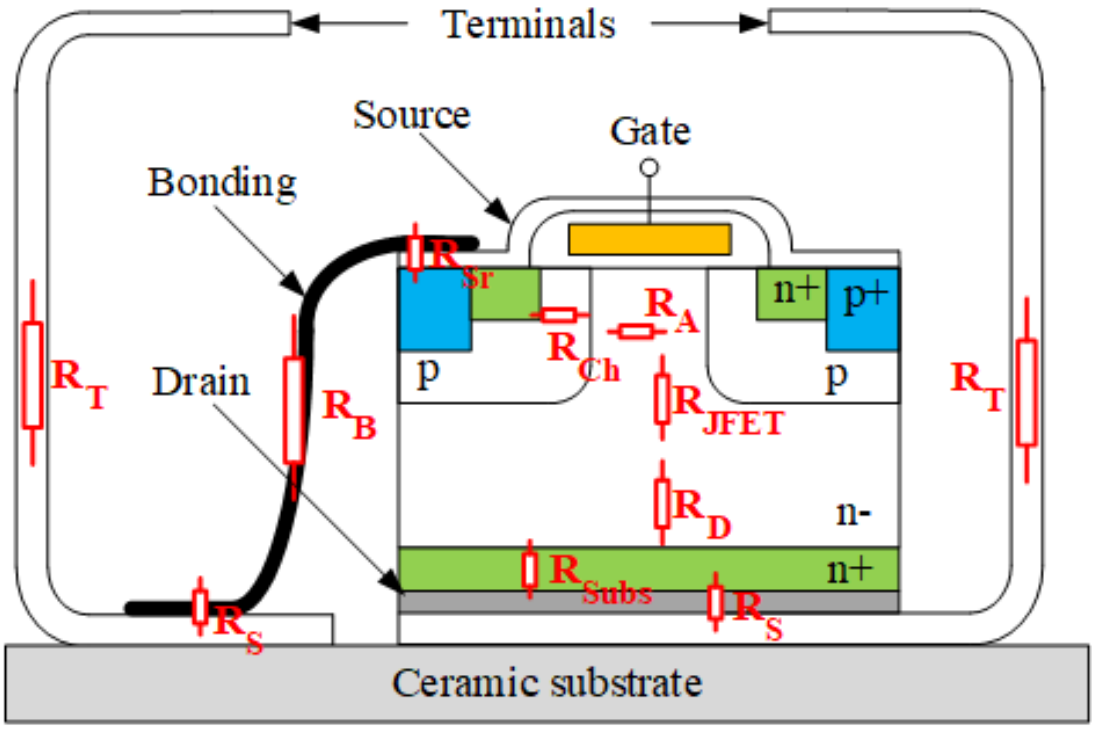


Figure 20. Simplified diagram of encapsulated power MOSFET with marked chosen physical components of On-state Channel Resistance ($R_{DS_{ON}}$) [86, 159].

However, the first strategy was not used in presented study, which is further discussed in section 3.2.2, while the second one is suitable only for the CC test, as V_{DS} across DUTs remains constant during the PC test.

Another aspect of proper EoL criteria definition is cost efficiency and overall price of the ALT. Thus, health indicators presented in previous paragraphs were critically evaluated in scope of a DtC methodology [66]. The main challenge related to $I_{GS_{LKG}}$, $I_{DS_{LKG}}$, $V_{GS_{TH}}$ or $Z_{TH_{JC}}$ monitoring, is rather impractical realization of the measurement procedure for a large number of tested samples. Accurate and valuable measurements require the usage of sophisticated (e.g. curve tracer) or custom made (e.g. setup for thermal impedance measurement) equipment and disassembling the samples from the laboratory setup. The usage of a curve tracer, instead of a source meter unit or a high precision current source with high precision voltage meter may significantly increase the investment cost of the ALT. Moreover, a complicated health indicator measurement procedure can significantly increase the maintenance cost in the large-scale ALT. In contrast to the health indicators

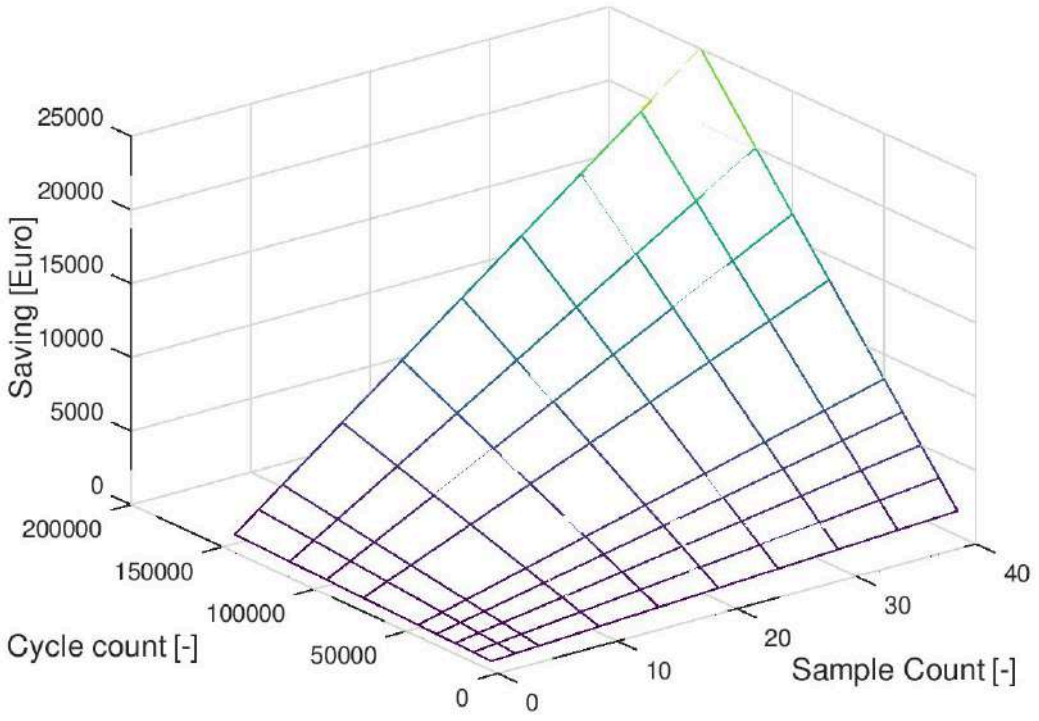


Figure 21. Model of maintenance cost difference for simple and complex health measurement in the scope of samples of MOSFETs tested and test duration (cycles) [86].

mentioned above, $R_{DS_{ON}}$ and V_{FWD} measurement circuits can be implemented directly in the test bench for PC test, which makes these health indicators more suitable for large-scale tests.

The impact of a chosen health monitoring strategy on the overall maintenance cost of the ALT test is depicted in Fig. 21. For the cost estimation it was assumed that a four wire measurement of $R_{DS_{ON}}$ and V_{FWD} takes approximately 1 *min* for a single sample, while dismounting the tested MOSFET from the laboratory setup, measurement of the desired complex health indicator, and remounting it back in the laboratory setup takes at least 6 *mins*. In the model discussed, it is assumed that the health measurement procedure is performed at least once per 2000 cycles and the cost of a working hour is 100 €. The presented simulations show that although the health monitoring strategy has no significant impact on the overall maintenance cost for small test batches ($\leq$ 10 samples) or short tests ($\leq$ 70000 cycles), for large test batches a proper decision on the

monitored health indicator may allow for savings reaching 25000 €. Code used for these calculations is given in listing below. Variables used in this code are following:

- s - number of tested samples,
- T - number of power cycles performed by devices during the test,
- $t1$, $t2$ - time required for measurement of simple (t1) and complex (t2) health indicator,
- h - cost of working hour,
- $CM1$, $CM2$ - maintenance cost of test assuming simple (CM1) and complex (CM2) health indicator measurement,
- CMd - savings.

```
s = [1, 3, 5, 10, 15, 20, 25, 30, 35, 40];
T = [10000, 20000, 30000, 40000, 50000, 80000, 100000, 120000,
   150000];
T1 = T./2000;
t1 = 1;
t2 = 6;
hcost = 100;
for i = 1:columns(T)
    for j = 1:columns(s)
       CM1(i,j) = 0;
       CM2(i,j) = 0;
       CMd(i,j) = 0;
    endfor
endfor
for i = 1:columns(T)
    for j = 1:columns(s)
       CM1(i,j) = T1(1,i)*t1*(hcost/60)*s(1,j);;
       CM2(i,j) = T1(1,i)*t2*(hcost/60)*s(1,j);;
    endfor
endfor
for i = 1:columns(T)
    for j = 1:columns(s)
       CMd(i,j) = CM2(i,j) - CM1(i,j);
    endfor
endfor
```

3.1.3 Control and health monitoring methods for large-scale Accelerated Lifetime Test (ALT)

Another issue is scaling up the batch size to decrease the confidence boundaries of the obtained reliability model, while maintaining the simplicity and low overall cost of the laboratory setup. All DUTs subjected to the ALT can be connected in parallel or in series. In the case of high current devices, parallel connection is not an optimal solution as it requires the usage of extremely high current to heat up the tested devices properly. The parallel connection of 1200 V 70 A SiC MOSFETs, chosen for discussed ALT, would require power supply with enormous current efficiency: from 2.2 kA for 40 DUTs, up to 6.6 kA for 120 DUTs. Practical realization of such a laboratory setup would require the usage of multiple high power DC sources, which would significantly increase the investment costs.

To overcome this issue, and decrease required current efficiency of power supply used in the laboratory setup to the reasonable level (e.g. $\sim$ 70 A), the sequential switching of DUTs can be introduced. As presented in Fig. 22, for such control strategy only one DUT is supplied at the same time. The main drawback of this approach is the extension of the cycle period by a factor of the batch size, which makes the whole test pointless. E.g. for base cycle period 20 s, 50000 power cycles performed in sequential switching of 40 DUTs would take $\sim$ 15 months.

Another disadvantage of the parallel connection is current sharing between the tested samples. In the case of SiC power MOSFETs, $R_{DS_{ON}}$ is $30 - 40$ $m\Omega$, which is very close to the resistance of wires and cables connecting DUTs. Thus, any asymmetry in galvanic connection between samples can cause unequal current sharing. Such phenomena can be avoided by a proper control strategy, like sequential switching discussed in previous paragraph or active current equalizing.

Series connection of the samples tested naturally solves the issues described above. Although, both voltage (for series connection) and current (for parallel connection) equalizing may be performed by actively adjusting the gate voltage, the precise drain-source voltage measurement is far more economical to implement, than the precise current

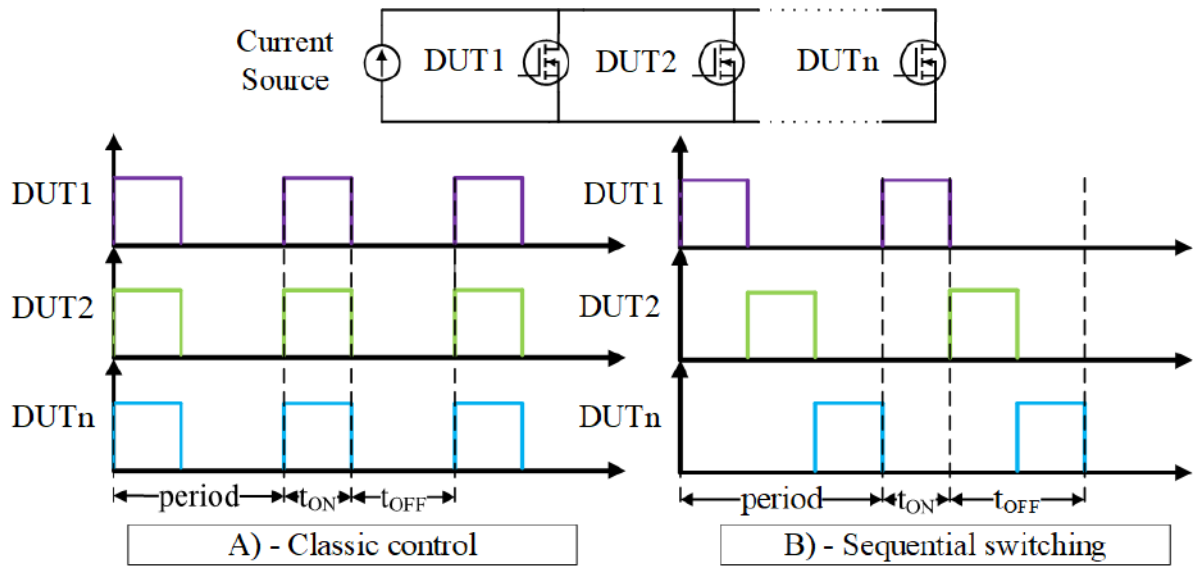


Figure 22. Comparison of classic control mode (on the left) and sequential switching (on the right) for Accelerated Lifetime Test (ALT) [86].

measurement. As working current during either PC or CC test consists only from direct component, it is impossible to use simple transducer for current measurement. Thus, either current shunt or Hall-effect current sensor would have to be used. However, high-accuracy high current shunts has rather large footprint in comparison to power MOSFET in $SOT-227B$ housing, which significantly limits the amount of DUTs, which could be placed on the same heatsink.

The next technical issue is the definition of a proper active heating method. Based on the electrical parameters of the tested SiC MOSFETs (see Tab. 3), the minimum DC current required to heat up the structure by $80°C$ is 62 A, which barely fits inside the transistor SOA. As the maximum rated current for tested samples is 68 A at Baseplate Temperature (T_C) of $25°C$, a test conducted with a higher temperature swing (e.g. $105°C$), would imply operation besides SOA - especially for higher Ambient Temperatures (T_A) (e.g. $30°C$ or $50°C$). Unfortunately, operation beside SOA may distort the test result, by false accelerating fatigue-like failure modes [117], which makes this approach sub-optimal.

Another possible solution for increasing the power dissipated at those MOSFETs to the desired level, e.g. 200 W, is to introduce high frequency switching losses. Hard switching

Table 3. *SiC* Power MOSFET electrical parameters

Electrical Parameter	I_{DS}	V_{DSS}	$R_{DS_{ON}}$	$Z_{TH_{JC}}$	$T_{J_{MAX}}$
Nominal Value	68 A	1200 V	34 $m\Omega$	0.6 $\frac{K}{W}$	175 $°C$

allows for working within the safe operating area, while sustaining the desired temperature swing. The main drawback of this approach is the high complexity of the laboratory setup, as a accurate switching losses estimation requires phased, fast, high-resolution voltage and current measurements [163]. Practical realization of such a measurement circuit requires the usage of expensive ultra-fast acquisition systems [164], which significantly increases the cost of the ALT procedure. Hard switching may also distort the test results by introducing new failure modes, e.g. parasitic Bipolar Junction Transistor (BJT) transistor turn-on [165] or power MOSFET self turn-on [166].

Based on the presented evaluation, the linear mode operation and heating up devices by limited DC current (e.g. $\sim 22.5\ A$ or $\sim 40\ A$), is found as an optimal and most economical solution. Unfortunately, such approach brings up concerns if linear mode operation will not distort the ALT results. Some researchers indicates that linear operation may cause uneven current distribution across structure, resulting in hot spots which significantly accelerate degradation mechanisms. However, the proper question shall be stated "does DUT has negative or positive thermal coefficient?". If the device is fully saturated, the transistor drain current may have a negative or a positive temperature coefficient, depending on the actual V_{GS} value, which may lead to the thermal instability [167]. However, operation of the power MOSFET in linear region assures negative thermal coefficient, which assures stable operation of power MOSFETs during ALT. By analogy, the AQG-324 guideline [155] obliges designer of the ALT of IGBTs to assure operation within the saturation area only, which corresponds to the power MOSFET linear (ohmic) region. Therefore, operation in linear region is found suitable for the ALT of *SiC* power MOSFETs. The graphical comparison of power MOSFET and IGBT output characteristics is presented in Fig. 23.

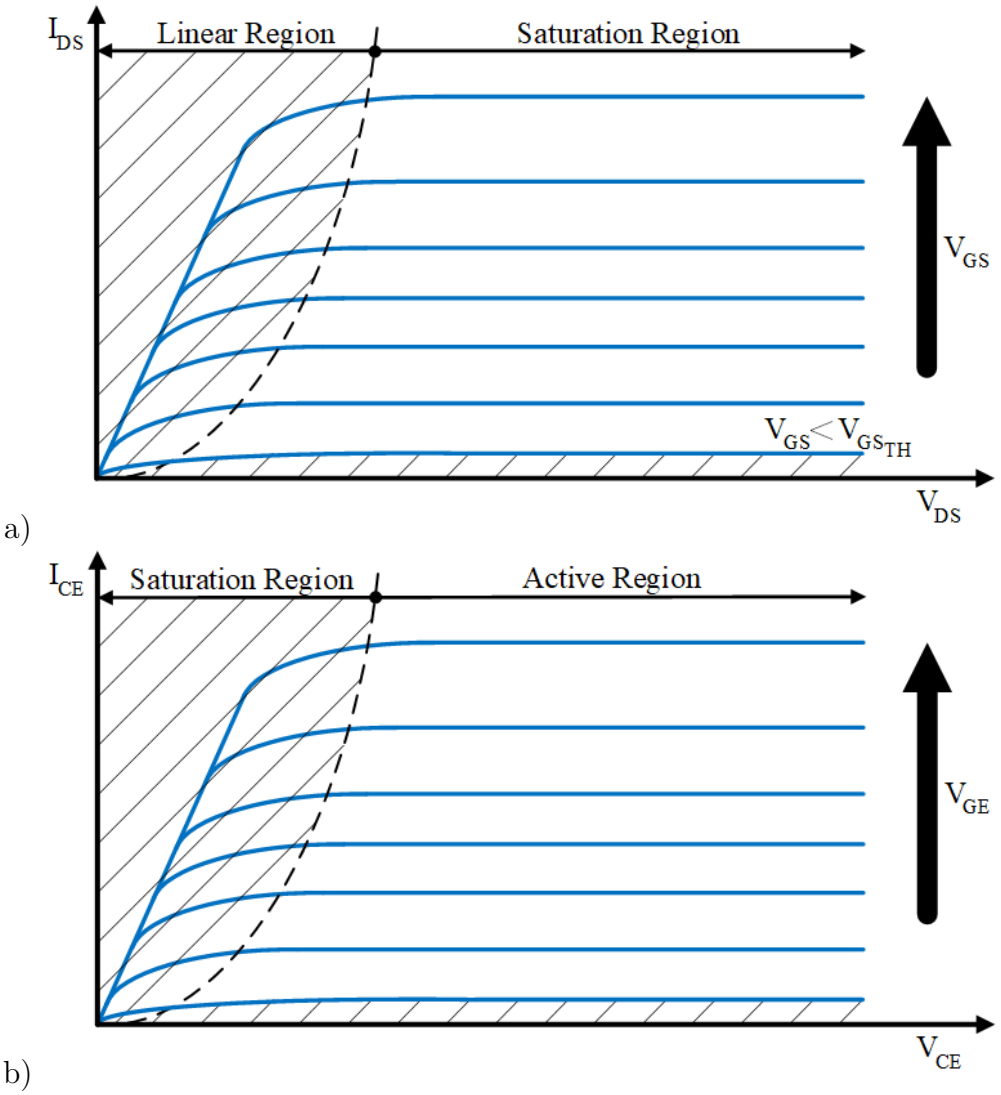


Figure 23. MOSFET a), and IGBT b) output characteristics with marked active, linear and saturation region [168].

3.2 Accelerated Lifetime Test (ALT) laboratory setup for encapsulated discrete SiC power MOSFETs

If testing strategy is a foundation of the ALT, its practical realization is a real engineering challenge. It requires to solve many technical issues, like: accuracy of Junction Temperature (T_J) estimation, stability of controller circuit, failure detection and others. Unfortunately, such technical aspects have significant impact on the ALT itself, test results

and utility of reliability model, prepared based on the obtained data. As presented in [169], a 5% temperature measurement error for $80°C$ temperature swing may introduce over 31% relative error in the lifetime estimation. Moreover, there are multiple factors which affect the overall temperature measurement error. Thus, in this section a key technical aspects of the ALT setup are discussed: the repeatability, the stability and the accuracy.

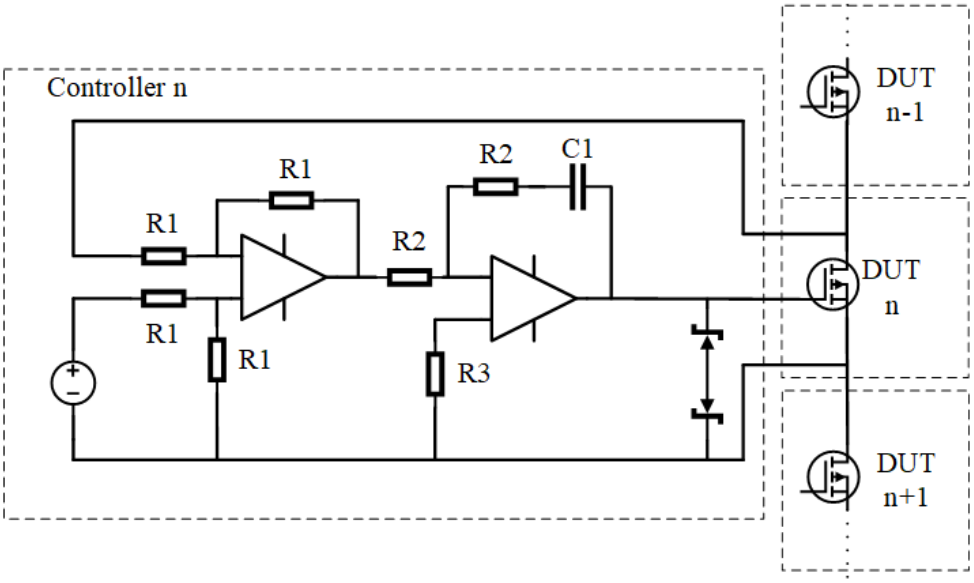
Various researchers have presented their proposals for laboratory setups for PC [170], TC [171] or Temperature and Power Cycling (TPC) [172]. A common feature for all of these laboratory setups is the small batch size - sample size varied from 1 to 10 samples [173, 174]. In contrast to the above, the laboratory setup presented in this thesis allows for simultaneous test of 12 different batches, which resulted in a total capacity of 120 samples. Also, previous research was mostly focused on high voltage IGBT modules and low power discrete semiconductors in common packages - e.g. $TO-220$, $TO-247$ [129, 147, 175]. The laboratory setup developed for purposes of this research well complements the above mentioned state-of-the-art, as it is optimized for a cost effective, large scale PC test of discrete semiconductors in industry grade housing: $SOT-227b$.

3.2.1 Controller for the Power Cycling test

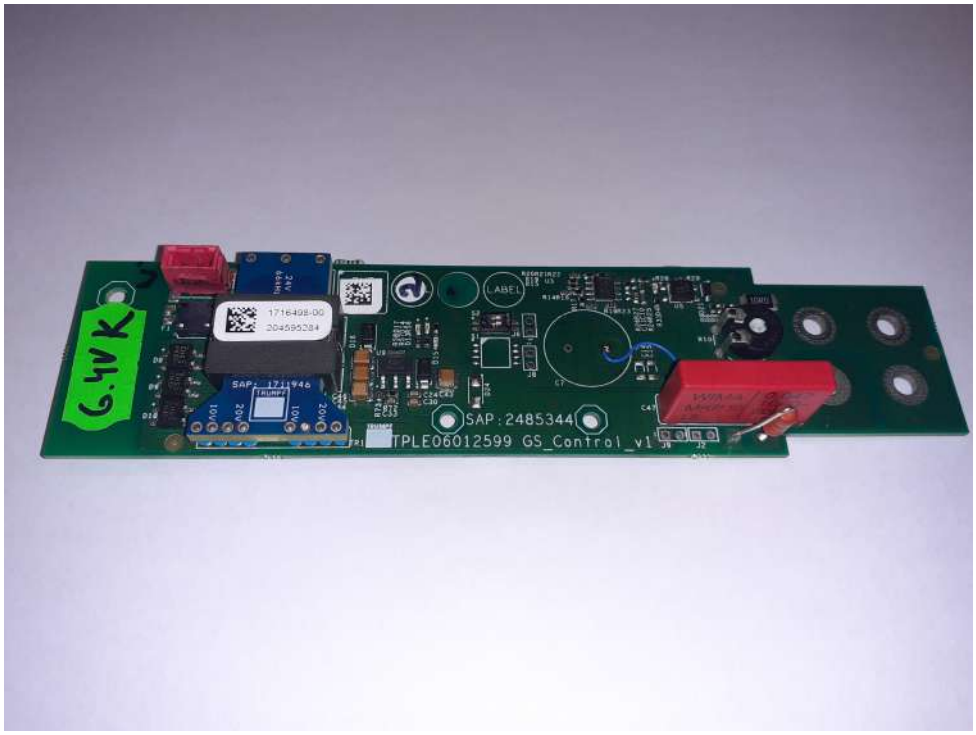
The first key requirements for the PC test bench is safety of staff working in the laboratory. The second one is a precise control of the DUTs Drain-Source Voltage (V_{DS}). Thus, the control circuit designed for this purpose has to fulfill following functional requirements:

- low temperature drift,
- great immunity for the electromagnetic noise - both transmissioned and radiated,
- high control and measurement repeatability.
- high control and measurement accuracy,
- galvanic isolation between DUT and accessible parts.

A schematic view and picture of the gate voltage controller circuit are presented in Figs. 24a) and 24b) respectively. All elements used in this circuit, have low thermal drift (25 ppm). Moreover, components marked in schematic view have following values: $R1 = 56\ [k\Omega]$, $R2 = 10\ [k\Omega]$, $R3 = 0\ [\Omega]$, $C1 = 47\ [nF]$. PCB was designed in such



a)



b)

Figure 24. Schematic diagram of the gate voltage controller circuit a) and corresponding top view of the assembled board b) [86]. Redundant components were removed from depicted Printed Circuit Board (PCB).

manner to ensure space for modifications, like increasing input capacitance of gate voltage controller. Thus, not all components needed to be assembled to ensure proper operation, as in the case of the PCB depicted in Fig. 24b).

Analysis of the PC test principle, indicates that the dispersion of the $T_{J_{MAX}}$ between DUTs may have influence on the reliability model prepared based on the ALT results. As it was proved during the laboratory testing, there are two possible sources of the T_J dispersion:

- Output Power Ripples ($P_{OUT_{RPL}}$) caused by the power supply itself and,
- Drain-Source Voltage Dispersion Between Neighboring Samples ($V_{DS_{(n)-(n+1)}}$) caused by tolerances of passive and active elements in the drain-source voltage controllers.

The first was measured with an MDO 3040 digital oscilloscope and a $TA-042$ differential probe, with 2% basic accuracy, while the second was measured with both a differential probe and a high precision voltmeter - $FLUKE$ 289, with 0.025% basic accuracy. Despite the high Output Voltage (V_{OUT}) and Drain-Source Current (I_{DS}), overall Voltage and Current Ripples ($V_{OUT_{RPL}}$, $I_{DS_{RPL}}$) across MOSFET cascade are very low and introduces minor power fluctuations. Those fluctuations are approximately 12 W, which causes an $0.18°C$ Junction Temperature Ripples ($T_{J_{RPL}}$). The V_{DS} dispersion was measured with the differential probe, and it is below 300 mV, which results in 6.75 W power loss deviation between DUT_n and DUT_{n+1}. This deviation causes 2.68 W Power Loss Dispersion Between Neighboring Samples ($P_{L_{(n)-(n+1)}}$), which corresponds to $\sim$ 4 $°C$ Junction Temperature Dispersion Between Neighboring Samples ($T_{J_{(n)-(n+1)}}$). Unfortunately, closer analysis of the test results showed that the noise itself recorded with a $TA-042$ differential probe was $\sim$ 240 mV, which resulted in very high signal to noise ratio - 0.8. Thus, this measurement was repeated with the $FLUKE$ 289 multimeter. The second round of measurement showed that the worst-case V_{DS} difference between samples is 96 mV for sampleset A, 119 mV for sampleset B, 32 mV for sampleset C, and 34 mV for sampleset D, resulting in $\sim 1.3°C$, $\sim 1.6°C$, $\sim 0.43°C$ and $\sim 0.46°C$ respectively. Therefore, this deviation is considered negligible, similarly to the deviation caused by the power ripples. This discussion is summarized in Tab. 4.

The test bench was retrofitted after 63355 of power cycles in order to increase its capacity and to address concerns given by manufacturer of tested SiC MOSFETs. After presenting initial test results, published in [86], to the manufacturer of discussed SiC

Table 4. Electrical parameters of the laboratory setup for the Accelerated Lifetime Test (ALT)

Batch Size	V_{OUT}	I_{DS}	P_{OUT}
40 $[pcs]$	260 $[V]$	22.5 $[A]$	5.8 $[kW]$
Sampleset Size	$V_{OUT_{RPL}}$	$I_{DS_{RPL}}$	$P_{OUT_{RPL}}$
10 $[pcs]$	12 $[V]$	1 $[A]$	12 $[W]$
$V_{DS_{(n)-(n+1)}}$	$P_{L_{(n)-(n+1)}}$	$T_{J_{RPL}}$	$T_{J_{(n)-(n+1)}}$
300 $[mV]$	2.68 $[W]$	0.18 $[°C]$	1.6 $[°C]$

Figure 25. View of laboratory setup before a) and after b) the retrofit [86]. In original test bench all samples were placed in the same rack system. After the retrofit, samplesets B and C were placed in the rack system on the left, while A, D and J were tested in the rack system on the right.

MOSFETs, he suggested that testing strategy is incorrect. Manufacturers statement was that operation in the linear mode, may shorten actual useful lifetime of tested devices. To verify this suggestions, following approach was introduced:

- the operating conditions for two samplesets (A and D) were changed, to increase V_{GS} while keeping the same Dissipated Power (P_L) per sample,
- the reference sampleset J was introduced.

If chosen operating conditions (I_{DS}, V_{DS}, V_{GS}) had no significant impact on degradation mechanism, nothing should change. Otherwise, increase of I_{DS} by factor of 2 should prolong DUTs useful lifetime, thanks to shifting operating conditions closer to active region.

Table 5. Operating conditions of tested semiconductor devices: nominal values [86].

Sample set no.	P_L $[W]$	ΔT_J $[°C]$	$T_{J_{MIN}}$ $[°C]$	$T_{J_{MAX}}$ $[°C]$	I_{DS} $[A]$
A	150.5	90.5	30	120.5	$22.5 \implies 40$
B	175	105.3	50	155.3	22.5
C	126	76.5	50	126.5	22.5
D	126	76.5	30	106.5	$22.5 \implies 40$
J	175	105.3	30	135.3	40

Table 6. Operating conditions of tested semiconductor devices: dispersion[86].

	P_L $[W]$		ΔT_J $[°C]$		$T_{J_{MAX}}$ $[°C]$	
	Mid-range	+/-	Mid-range	+/-	Mid-range	+/-
A	150.66	0.43	90.40	0.26	120.40	0.26
B	174.95	1.34	104.97	0.80	154.97	0.80
C	126.91	0.39	76.14	0.24	126.14	0.24
D	127.64	0.36	76.58	0.22	106.58	0.22
J	175.16	2.04	105.09	1.22	135.09	1.22

Moreover, ALT was also repeated by manufacturer. Their test results were shown to TRUMPF and compared with research presented in this thesis. However, manufacturer classified their ALT as *confidential*, thus their test procedure nor their test results can not be discussed in this thesis.

As depicted in Fig. 25, the main difference between initial and retrofitted test bench is mechanical design, which allows to add additional sampleset (J) in the retrofitted test bench. Same as in the case of the initial setup, $V_{DS_{(n)-(n+1)}}$, $T_{J_{(n)-(n+1)}}$ and T_J accuracy caused by power fluctuations, were measured during start up of the ALT.

The last key parameter of the gate voltage controller is its stability over time. Periodical V_{DS} measurements performed for each DUT at the very beginning of the ALT test, after 16928, 63415, 81871 cycles and later, showed that power MOSFET's operating conditions remained at the same level, within $\pm 100\, mV$ confidence boundaries. To sum up discussion in this subsection, operating conditions and their dispersion for DUTs are listed in Tab. 5 and Tab. 6.

3.2.2 Power MOSFET junction temperature estimation for Accelerated Lifetime Test (ALT)

The next technical issue in the ALT is an accurate T_J measurement. Both direct and indirect measurement methods were successfully utilized in [176, 177]. However, in the case of encapsulated power MOSFET, an accurate T_J measurement is especially challenging, as the utilization of any direct measurement method is impossible.

The main disadvantage of the indirect temperature methods is a rather small change of the measured signal with temperature [178]. This fact significantly increases the complexity and price of equipment used for T_J estimation based on the Thermo-Sensitive Electrical Parameter (TSEP) monitoring. In addition, power MOSFET TSEPs (e.g. $R_{DS_{ON}}$, $V_{GS_{TH}}$, $I_{DS_{LKG}}$, etc.) changes as chip and bond wire degradation progresses. This fact is especially unfortunate as an accurate T_J estimation requires a periodic calibration procedure, which could significantly increase the maintenance cost of the ALT.

For these reasons, a different approach has been chosen for the presented laboratory setup. Junction temperature is estimated based on monitored Baseplate Temperature (T_C), Dissipated Power (P_L) and known initial Junction-to-Case Thermal Impedance ($Z_{TH_{JC}}$). As stated previously, thermal impedance changes over time due to degradation of soldering between either chip and paddle or paddle and baseplate. Therefore, this method allows to determine only the initial conditions - e.g amplitude of junction temperature swing for fresh samples. This is completely sufficient for purposes of presented ALT, as it was designed for empirical reliability model extraction and the self-acceleration of the degradation mechanism is a desired phenomenon. Thus, for purposes of reliability modelling only an initial temperature swing amplitude and absolute junction temperature are required, as it results in the useful lifetime of SiC power MOSFET defined as a number of power cycles, for a given initial ΔT_J. Thus, to estimate T_J following equation can be used:

$$T_J = P_L \cdot Z_{TH_{JC}} + T_C \tag{13}$$

The main drawback of the model-based T_J estimation is the strong relationship between thermal model parameters, environmental conditions and the placement of the reference

temperature sensor [179]. One possibility to overcome this flaw, and to increase T_J estimation accuracy is measurement and identification of $Z_{TH_{JC}}$ parameters (e.g. with a particle swarm optimization algorithm [180]), for a sample placed in the ALT laboratory setup. Such approach allows to easily improve accuracy of T_J estimation for initial conditions, at the very beginning of ALT test. However, if it is desired to accurately monitor T_J during the test, this calibration procedure has to be repeated periodically to maintain estimation accuracy at a satisfactory level. Unfortunately, this significantly increases the maintenance cost of the ALT procedure. Another possible solution, for accurate T_J monitoring during ALT of power semiconductors, is the preparation of a complex, time-dependent thermal impedance model, which covers variations of lumped parameters caused by degradation or operating conditions, as presented in [181]. These flexible RC parameters can be extracted with Finite Element Modelling (FEM) and can be verified or calibrated with proper experiments. The main drawback of this method is the amount of time and effort spent on the identification of thermal model parameters, which increases the investment cost of ALT test.

An alternate approach is to prepare a reliability model based on the *case temperature* or *reference temperature* instead of the *estimated junction temperature*; however, such an approach difficult any attempts on comparative study between results obtained by different researchers. Therefore, it would only be useful for internal purposes of industrial consumer of power electronics - e.g. to estimate the UL of an SiC power MOSFET, based on actual stressors present in a target application. The main benefit of this approach is simplicity - as far as environmental parameters remain constant and case temperature is measured in the same way in ALT the laboratory setup and target application, the developed reliability model is correct. Environmental conditions in HPPS for plasma processing are usually stable, as they are hermetically sealed and water cooled, and also they are used in clean rooms, where either air or coolant temperature is strictly monitored. Thus, it is possible to model target environmental conditions in the ALT test setup, which makes proposed alternate approach for temperature measurement extremely delightful option, especially as the ALT presented in this thesis was prepared solely

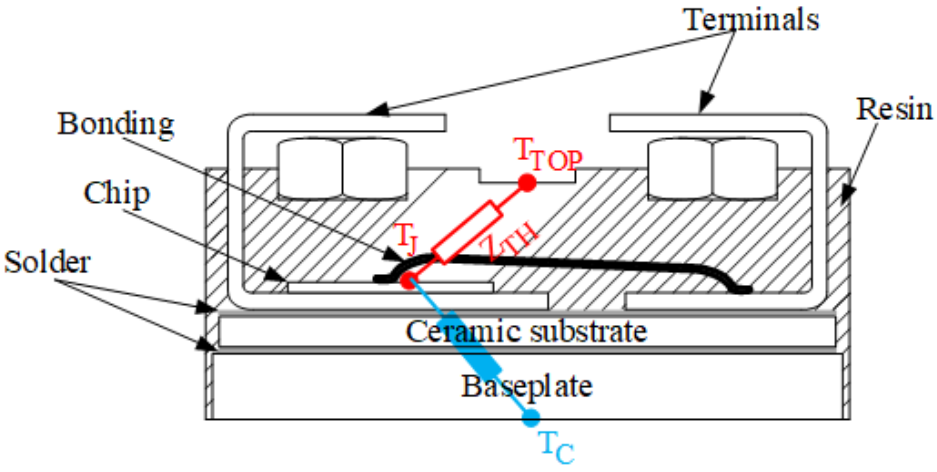


Figure 26. Simplified cross-section of semiconductor device in $SOT-227B$ housing. Junction temperature, case temperature and reference temperature of such device are labeled Junction Temperature (T_J), Baseplate Temperature (T_C) and Top Surface Temperature (T_{TOP}), respectively.

for internal purposes of TRUMPF. Temperature measurement circuit, designed for this purpose, was presented in [182]. Although importance of the *simplicity* of proposed strategy may not be clear if the ALT test itself is considered, it is critical for practical usage of developed reliability model. In many HPPS, it is impossible to perform either direct or TSEP-based T_J measurement, due to high operating frequency or packed design. Thus, any reliability assessment based on measurements performed in real HPPS, would be heavily affected not only by accuracy of reliability model, but also by accuracy of T_J estimation method used for identification of the stress level. Moreover, complex measurement methods introduces concerns about reproducibility, which may also affect results of further reliability predictions. Therefore, the *simplicity* is one key aspects defining the applicability of reliability model prepared for purposes of the proposed DfR procedure. Thus, during presented ALT beside T_C measurement, which was performed to estimate junction temperature for initial conditions, the temperature of DUT Top Surface Temperature (T_{TOP}) was also recorded. Graphical relationship between these reference temperatures is presented in Fig. 26.

3.2.3 Failure detection algorithm for the Accelerated Lifetime Test (ALT)

The last technical challenge related to the design of the ALT laboratory setup is failure detection. As discussed earlier, the test was conducted until all samples fail; therefore, it was necessary to design an emergency circuit, capable of shutting down the heating current within milliseconds in order to avoid complete destruction of the SiC chip. This allows for further analysis of a failed MOSFET - e.g. decapsulation or Röntgen Radiation (X-RAY) photography. For this purpose, a voltage and current monitoring circuit, presented in Fig. 27, was designed. An emergency algorithm based on both measurements determines

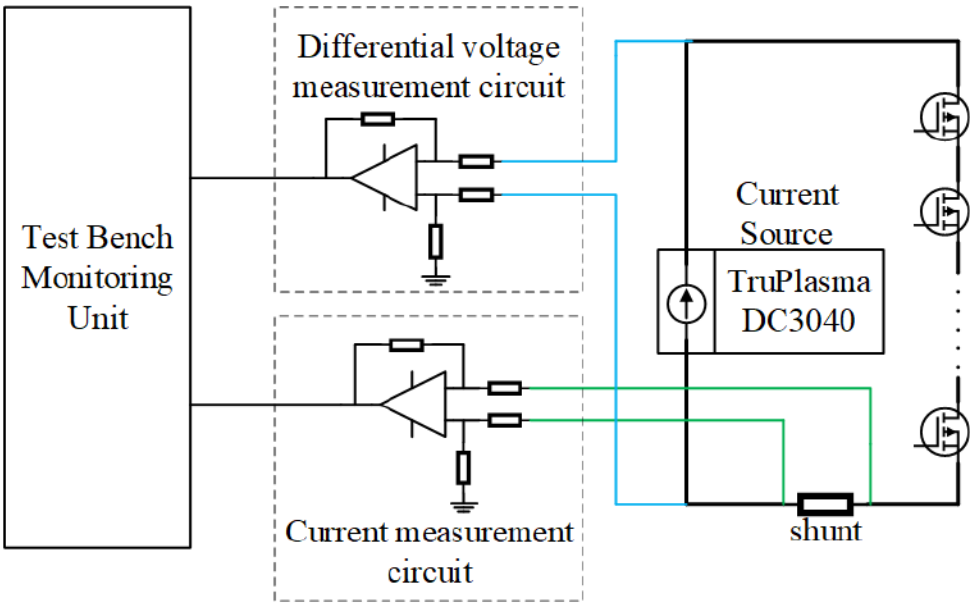


Figure 27. Schematic of supervisory circuit for failure detection.

the condition of the laboratory setup, and whether there is a heating pulse, short circuit or open circuit. Four different threshold levels for the voltage and current measured were defined:

- Current Threshold Low (I_{LOW}): $I_{NOMINAL} \cdot 5\%$,
- Current Threshold High (I_{HIGH}): $I_{NOMINAL} \cdot 90\%$,
- Voltage Threshold Low (V_{LOW}): $V_{NOMINAL} - V_{DS_{MIN}}$,
- Voltage Threshold High (V_{HIGH}): $V_{NOMINAL} \cdot 120\%$,

where Nominal Current ($I_{NOMINAL}$) is the RMS current value during a cycle, Nominal Voltage ($V_{NOMINAL}$) is the RMS voltage across the MOSFET cascade during a cycle and $V_{DS_{MIN}}$ is the Minimum Drain-Source Voltage in single DUT during the test. In the discussed emergency detection algorithm, Actual Drain-Source Voltage (V_{ACT}) and Actual Drain-Source Current (I_{ACT}) are constantly compared to these threshold levels, to detect three possible states: Short-Circuit (S_C), Open-Circuit (O_C) and Correct Operation (C_O). The logical relationships used for this purpose are presented by (14) - (16). In Fig. 28, an actual failure detection is presented. Both output current (channel 1 - yellow) and voltage (channel 2 - green) across the tested samples decrease exponentially after failure detection. As each voltage controller circuit is equipped with a parallel RC circuit, balancing voltage across MOSFETs, it is assured that neither failure has a negative impact on the rest of the tested samples.

$$I_{ACT} \geq I_{HIGH} \wedge V_{ACT} \leq V_{LOW} \implies SC = 1 \tag{14}$$

$$V_{ACT} \geq V_{HIGH} \wedge I_{ACT} \leq I_{LOW} \implies OC = 1 \tag{15}$$

$$SC \neq 1 \wedge OC \neq 1 \implies CO \tag{16}$$

The presented failure detection circuit may also be used for further automatization of the ALT test bench or integration of the laboratory setup in a larger infrastructure, compliant with *Industry* 4.0 concept [183]. In this thesis, the most basic version of the laboratory setup for ALT of power *SiC* MOSFETs is presented. Therefore, each failure stops the test until the operator manually removes the failed sample and resets the alarm, which takes $\sim 15\ min$.

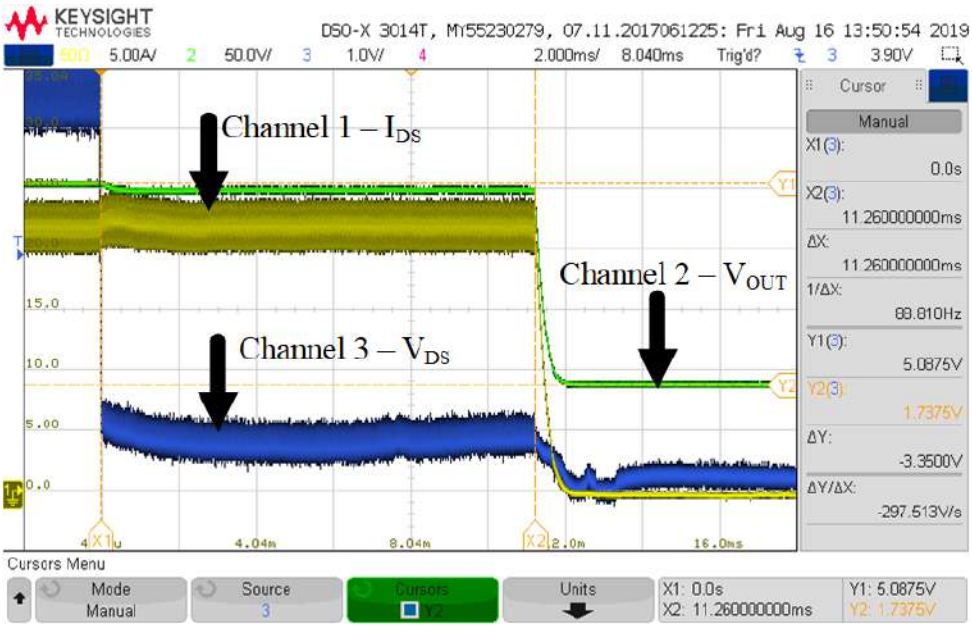


Figure 28. Test of MOSFET failure detection circuit: Channel 1 - operating current (I_{OUT}), Channel 2 - voltage at MOSFET cascade (V_{OUT}), Channel 3 - voltage at shorted sample (V_{DS}) [86]. Test was performed at DUT #8D.

3.3 Experimental verification

3.3.1 Health indicator measurements

The results of periodic health indicators measurements for tested power semiconductor devices are presented in Figs. 29 - 33.

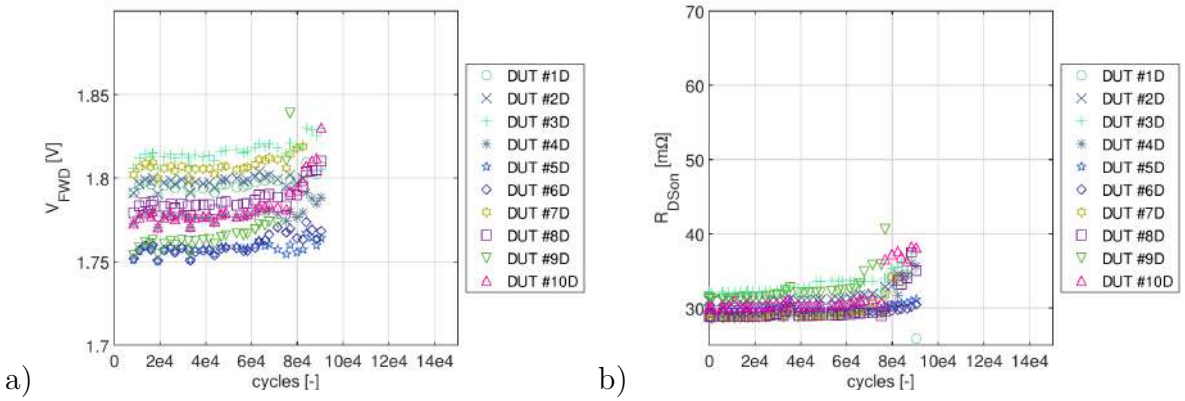


Figure 29. Body Diode Forward Voltage (V_{FWD}) drop a), and On-state Channel Resistance ($R_{DS_{ON}}$) b) measurement for sample set D - $\Delta T_J = 76.5°C$, $T_{J_{MIN}} = 30°C$, $T_{J_{MAX}} = 106.5°C$.

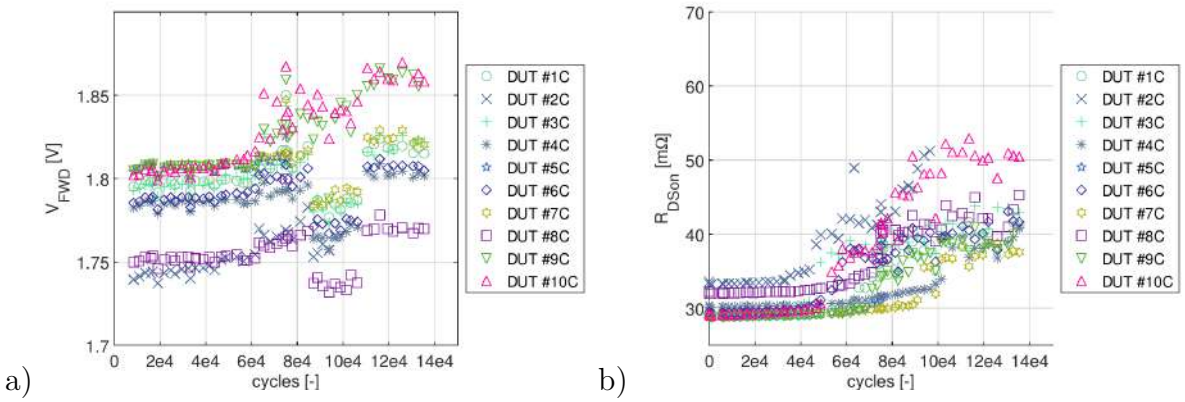


Figure 30. Body Diode Forward Voltage (V_{FWD}) drop a), and On-state Channel Resistance ($R_{DS_{ON}}$) b) measurement for sample set C - $\Delta T_J = 76.5°C$, $T_{J_{MIN}} = 50°C$, $T_{J_{MAX}} = 126.5°C$.

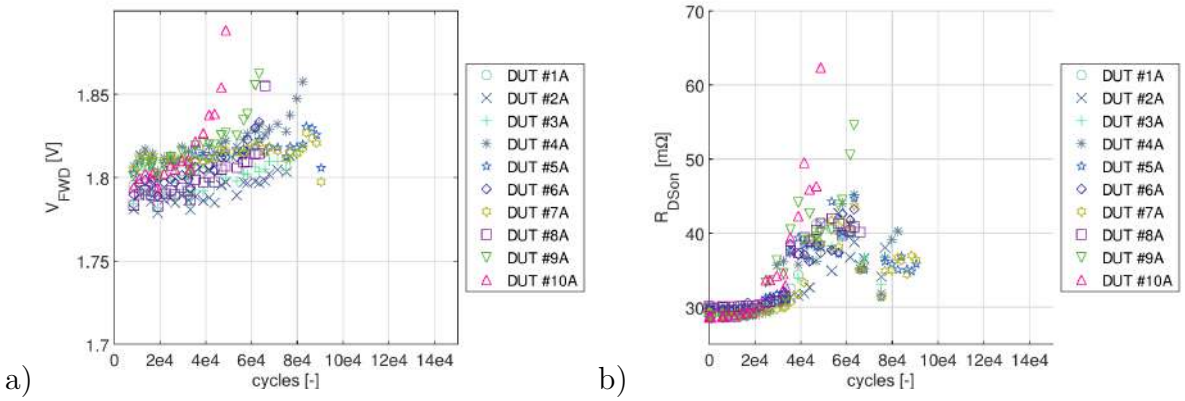


Figure 31. Body Diode Forward Voltage (V_{FWD}) drop a), and On-state Channel Resistance ($R_{DS_{ON}}$) b) measurement for sample set A - $\Delta T_J = 90.5°C$, $T_{J_{MIN}} = 30°C$, $T_{J_{MAX}} = 120.5°C$.

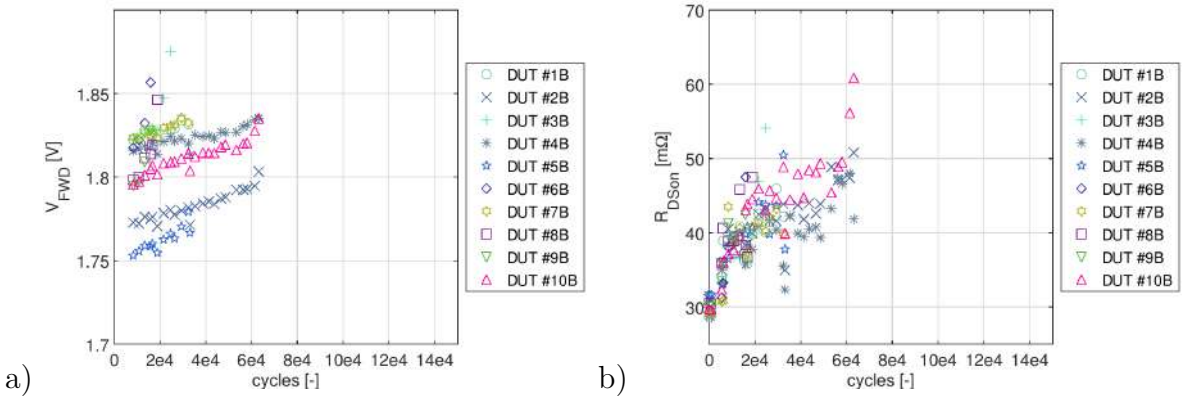


Figure 32. Body Diode Forward Voltage (V_{FWD}) drop a), and On-state Channel Resistance ($R_{DS_{ON}}$) b) measurement for sample set B - $\Delta T_J = 105.3°C$, $T_{J_{MIN}} = 50°C$, $T_{J_{MAX}} = 155.3°C$.

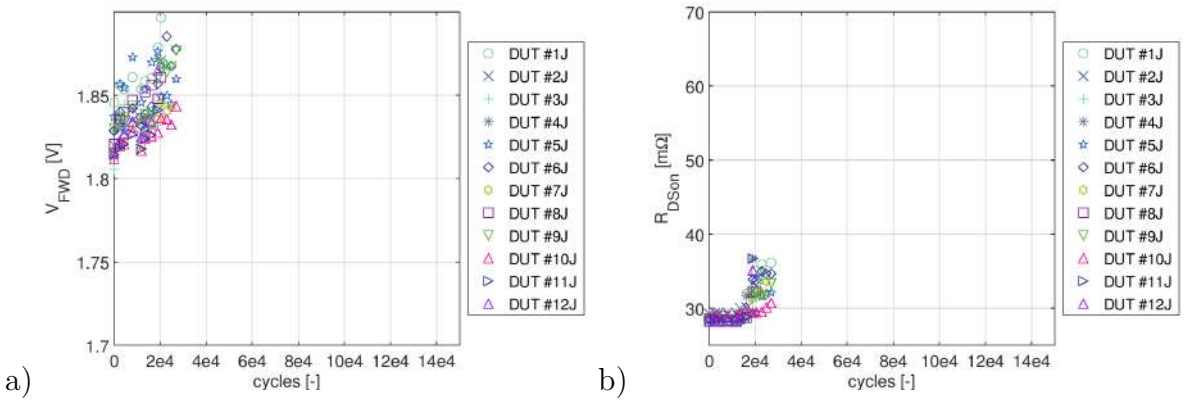


Figure 33. Body Diode Forward Voltage (V_{FWD}) drop a), and On-state Channel Resistance ($R_{DS_{ON}}$) b) measurement for sample set J - $\Delta T_J = 105.3°C$, $T_{J_{MIN}} = 30°C$, $T_{J_{MAX}} = 135.3°C$.

In the case of the power MOSFETs, which were subjected to low thermal stress (ΔT_J swing from $30°C$ to $106.5°C$ per cycle), neither of health indicators showed any signs of degradation in the first 40000 cycles. A deeper analysis of Fig. 29, shows significant increase of $R_{DS_{ON}}$ after $70000 - 80000$ cycles, which corresponds to proper increase of V_{FWD}. Such phenomena clearly indicates progressing degradation of SiC power MOSFET. Although, the total increase of $R_{DS_{ON}}$ before failure varied among samples: from $3\% - 4\%$ for DUTs $\#5D$ and $\#6D$, up to $29\% - 26\%$ for DUTs $\#9D$ and $\#10D$. Devices from group C earlier showed signs of degradation, the clear increase of $R_{DS_{ON}}$ was visible after only 50000 cycles, although the corresponding increase of V_{FWD} was found after 10000 cycles later.

In comparison to groups C and D, health indicators measured for power MOSFET subjected to moderate thermal stress ($90.5°C$ junction temperature swing), shows a clear drift after only 40000 cycles. Similarly to the previously discussed groups, both electrical parameters changed in the similar time, which suggests a rapidly progressing degradation or even a lift off of the bond wires in the tested semiconductor devices. The $R_{DS_{ON}}$ measurement for DUT $\#10A$ increased over 100% from its nominal value during ALT.

In contrast to above discussed results, health indicators of DUTs subjected to heavy thermal load (B, J) indicates rapidly progressing degradation from the very beginning of the ALT. In the case of samples from group B, early change of electrical parameters is visible for both $R_{DS_{ON}}$ and V_{FWD}. However, for samples from group J $R_{DS_{ON}}$ did not

Table 7. Failures recorded during Accelerated Lifetime Test (ALT) test [184].

	group A	group B	group C	group D	group J
#1	63394	33163	–	92328	28973
#2	79651	63189	96526	82532	21451
#3	82532	24643	–	92328	24874
#4	82532	63189	–	92328	19157
#5	92328	33359	75037	92328	24727
#6	63404	16283	–	92328	28973
#7	92328	33100	–	82512	25719
#8	67710	18975	–	92328	22882
#9	63394	16756	133117	76829	28973
#10	48793	63189	–	91794	28973
#11	N/A	N/A	N/A	N/A	19686
#12	N/A	N/A	N/A	N/A	19536

change in the first 16000 - 20000 cycles. Similarly to groups C and D, devices subjected to lower operating current lasted longer, despite heavy degradation.

3.3.2 Post Failure Analysis

To verify if failures were indeed caused by *fatigue-like* failure modes, 32 random selected samples were subjected to post-failure analysis, which consisted of following steps:

1. electrical measurement,
2. X-RAY imaging,
3. Confocal Scanning Acoustic Microscopy (CSAM),
4. post-decapsulation visual inspection.

Post failure analysis was performed with cooperation of the Łukasiewicz Tele- and Radio Research Institute (ITR). First group of failed samples was subjected to the post failure analysis during retrofit of laboratory setup, while the second group was examined at the end of the ALT. As presented in Tab. 8, most failures resulted in both Gate-Source and Drain-Source shorted.

The next step of the post-failure analysis is a non-invasive laboratory testing - the X-RAY imaging and CSAM. In the case of the first group of samples (DUTs #7B,

Table 8. Electrical test results of failed SiC power MOSFETs.

Sample	$G-S$	$D-S$	Sample	$G-S$	$D-S$
$\#1A$	Shorted	Shorted	$\#1C$	-	-
$\#2A$	Short circuit to PE		$\#2C$	Shorted	$15k\ \Omega$
$\#3A$	Shorted	Shorted	$\#3C$	-	-
$\#4A$	Shorted	Shorted	$\#4C$	-	-
$\#5A$	Shorted	Shorted	$\#5C$	Open	Shorted
$\#6A$	Shorted	Shorted	$\#6C$	-	-
$\#7A$	Shorted	Shorted	$\#7C$	-	-
$\#8A$	Shorted	Shorted	$\#8C$	-	-
$\#9A$	Shorted	Shorted	$\#9C$	Shorted	Shorted
$\#10A$	2.2 Ω	Shorted	$\#10C$	-	-
$\#1B$	Open	Instable	$\#1D$	Shorted	Shorted
$\#2B$	Shorted	Shorted	$\#2D$	Shorted	Shorted
$\#3B$	Shorted	Shorted	$\#3D$	Shorted	Shorted
$\#4B$	Shorted	Shorted	$\#4D$	Shorted	Shorted
$\#5B$	Shorted	Shorted	$\#5D$	Shorted	Shorted
$\#6B$	Shorted	Shorted	$\#6D$	Shorted	Shorted
$\#7B$	4 Ω	3.5 Ω	$\#7D$	Shorted	Shorted
$\#8B$	Instable	Instable	$\#8D$	Shorted	Shorted
$\#9B$	Shorted	Open	$\#9D$	Shorted	Shorted
$\#10B$	Shorted	Shorted	$\#10D$	Shorted	Shorted
$\#1J$	Shorted	Shorted	$\#7J$	Shorted	Shorted
$\#2J$	Shorted	Shorted	$\#8J$	Shorted	Open
$\#3J$	Shorted	Shorted	$\#9J$	Shorted	Shorted
$\#4J$	Shorted	Shorted	$\#10J$	Shorted	Shorted
$\#5J$	Shorted	Shorted	$\#11J$	Shorted	Shorted
$\#6J$	Shorted	Shorted	$\#12J$	Shorted	Shorted

$\#1B$, $\#5B$, $\#8B$, $\#6B$, $\#10A$), neither X-RAY nor CSAM analysis showed any signs of delamination. As it was confronted with the supplier, cavities in the soldering beneath the semiconductor chip, visible in X-RAY images presented in Fig. 34, were within an acceptable range - typical for their manufacturing process. Thus, those cavities were not found as a result of the ALT. In addition to the above-mentioned, X-RAY scanning revealed also a crack in the SiC chip structure.

The second group of samples chosen for post-failure analysis was subjected only to CSAM analysis, which working principle is based on physics of acoustic wave. When wave propagates through any medium, it may be either scattered, absorbed or reflected at the interface between different materials. In this technique, the echo, generated by the acoustic impedance mismatch between two materials, is registered. Then, the image of tested sample is generated, based on the analysis of the time the ultrasonic pulse requires to reach the material interface and return to the transducer. This allows to determine magnitude and phase of reflected signal. Thus, this technique allows to find irregularities or discontinuities in any solid material, which have high penetration depth of acoustic waves. Depending on the axis and surface of scanning, A-scan, B-scan, C-scan and T-scan can be specified [185].

Bright areas in post-processed images are related to high magnitude of the reflected signal. Moreover, if the ultrasound beam goes from high acoustic-impedance medium to a low acoustic-impedance medium, it causes the inversion of the phase of the reflected beam. These two effects combined are typical for material-air interface, and therefore may indicate presence of delamination or voids, as depicted in Fig. 35. The CSAM imaging revealed severe solder delamination in 19 DUTs - in certain examples chip was completely detached from the metal paddle.

The last step of post failure analysis discussed in this thesis is microscopy analysis of the chemically decapsulated samples. The moulding was dissolved with concentrated Sulfuric Acid (H_2SO_4). As the decapsulation process itself is highly invasive, it was performed in two stages. First, a short acid bath allowed the lifted bond wires to be exposed (see Fig. 36), which confirmed the hypothesis that the observed growth of $R_{DS_{ON}}$ and V_{FWD} was

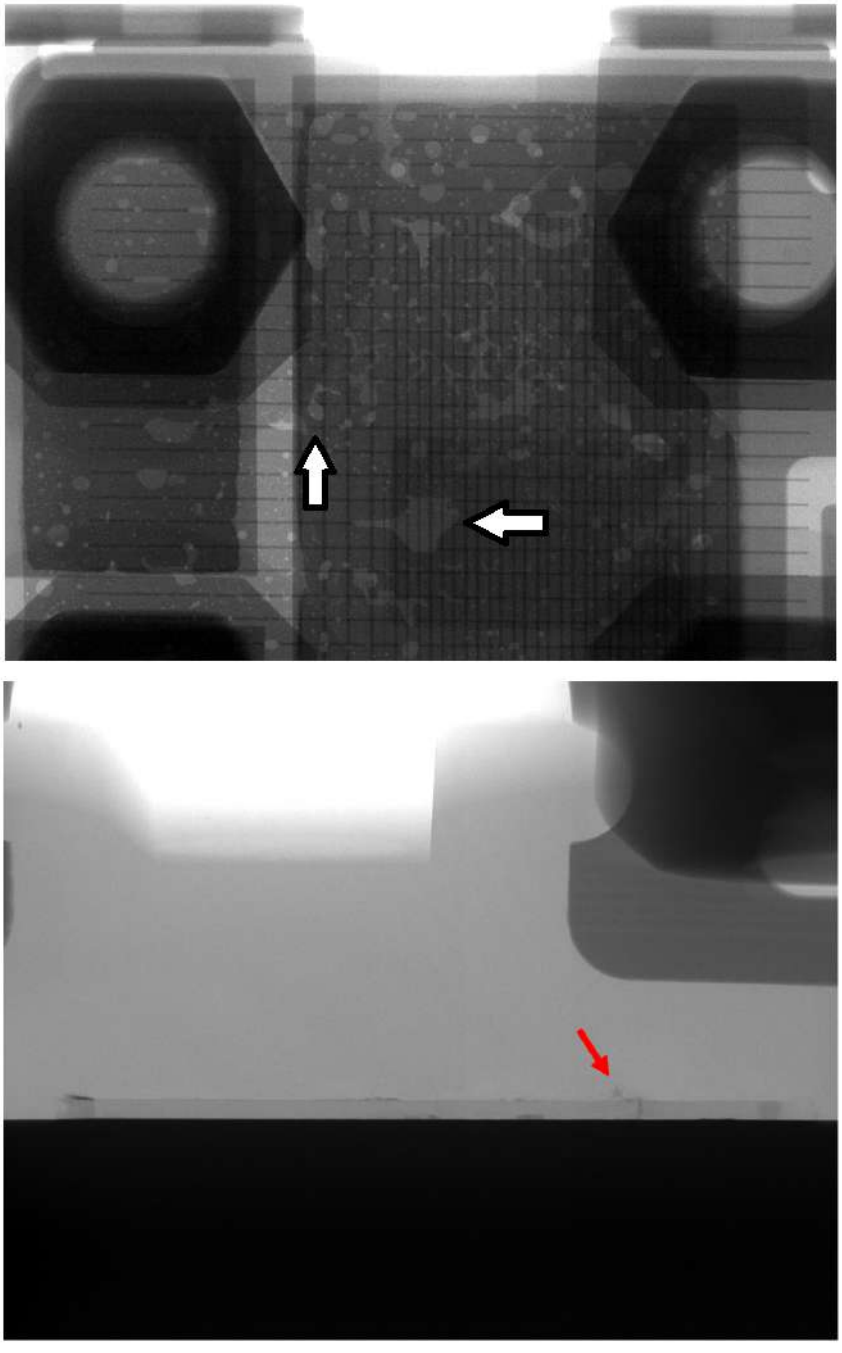


Figure 34. Top view a), and side view b) of a *SiC* Device Under Test (DUT) #10*A* subjected to X-RAY analysis. Visible small cavities (white arrows) were verified as typical of the manufacturing process - they were not induced by the Accelerated Lifetime Test (ALT) test. Crack in *SiC* chip, located beneath terminal, was marked with red arrow [86].

caused by the degradation of the bond wire connection. Among analyzed samples, over 24 DUTs had few or all bond wires lifted-off. Moreover, in single bond wire, the heel-crack

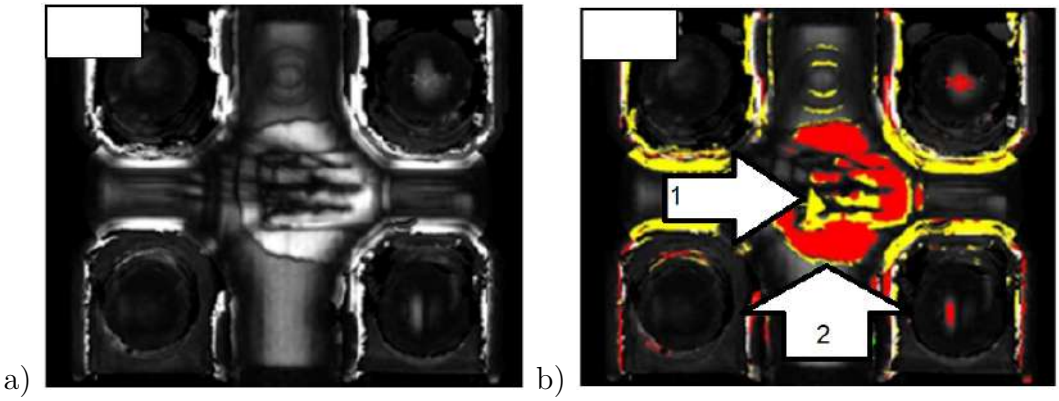


Figure 35. C-scan of Device Under Test (DUT) #9*J* subjected to the Confocal Scanning Acoustic Microscopy (CSAM) imaging. Bright areas indicates high magnitude of the reflected signal, while yellow and red areas indicates inversion of the phase of the reflected beam. These areas are marked with arrows 1 and 2 respectively. Presented data suggests severe delamination of soldering beneath the *SiC* chip.

was found (see Fig. 36b)). In some devices, although most of bond wires were lifted-off, the soldering beneath the chip remained intact (see Fig. 37). Second, a longer acid bath revealed the *SiC* chip and distinct black markings from the lifted bonding wires, depicted in Fig. 38a). This characteristic black mark is a result of the chemical reaction between sulfuric acid and either remains of solder or the intermetal dielectric layer. Unfortunately, further metallurgical analysis was impossible to perform due to the highly invasive nature of the decapsulation process. However, a comparison of the degraded power MOSFET with fresh sample, depicted in Figs. 38a)-b), supports this hypothesis, as each bond wire is surrounded with a characteristic black sediment.

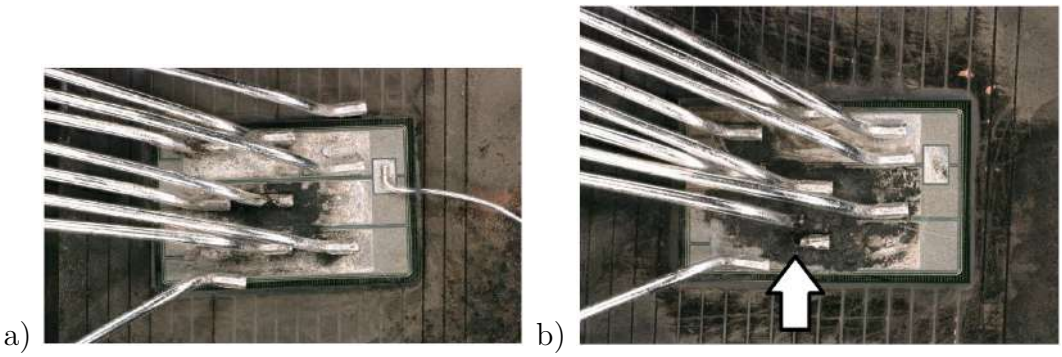


Figure 36. Top view of Device Under Test (DUT) #9*J* a), and DUT #6*J* b) after chemical decapsulation process. In both samples, some bond wires are lifted-off. A cracked bond wire is marked with white arrow [184].

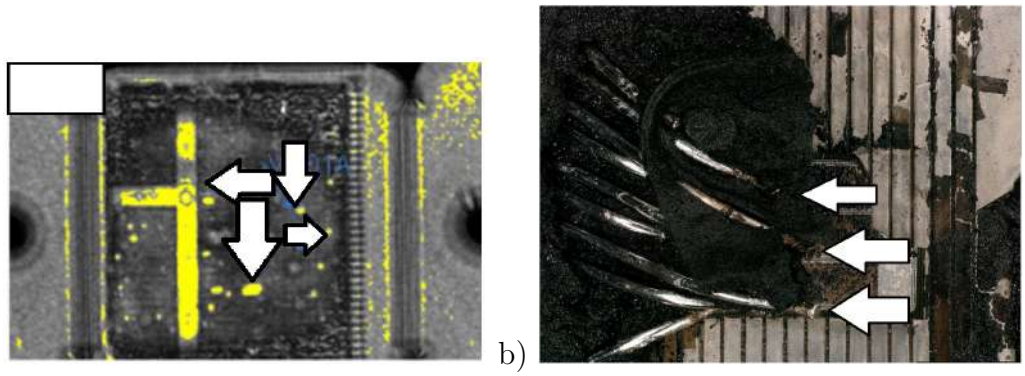


Figure 37. Bottom-up Confocal Scanning Acoustic Microscopy (CSAM) imaging a), and post decapsulation photography of Device Under Test (DUT) #5C . Minor voids and cavities, marked with white arrows in a), are not considered as rejectable according to the J-STD-020E standard, while clearly some of bond wires are lifted off. Lifted bond wires are marked with white arrows in b) [184].

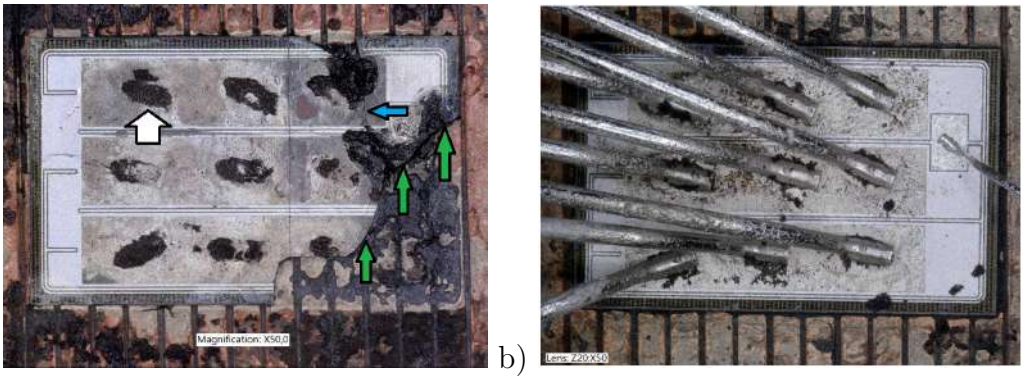
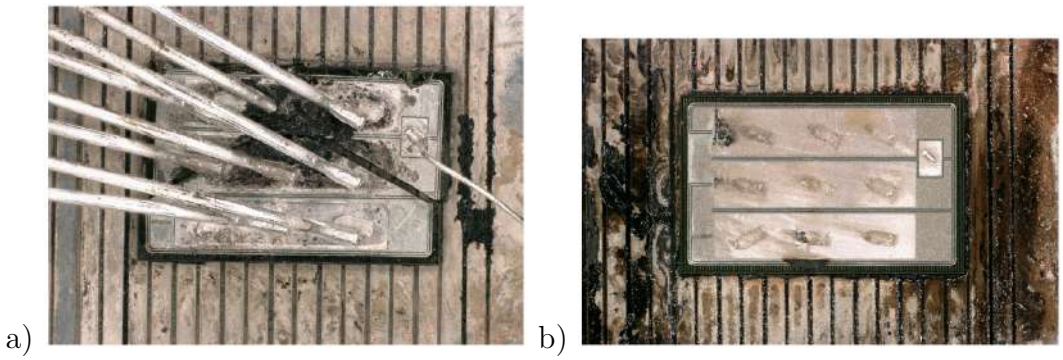


Figure 38. Top view of decapsulated Device Under Test (DUT) #10A after long acid bath a), and top view of fresh sample subjected to the same decapsulation process b). Visible black markings are left by lifted bonding wires (white arrow). Thin crack in SiC chip (blue arrow) is the result of a hotspot caused by non-laminar current flow across the SiC chip. The chip itself was partially damaged during the decapsulation process. It broke along the crack line (green arrows) [86].

As presented in Fig. 39, the X-RAY imaging and visual inspection of decapsulated device revealed also a crack across the SiC chip in some samples. However, in other devices, only a puncture damage of semiconductor structure was present. Either crack or puncture damage of SiC chip has the same root cause. With each lifted bond wire, the current is conducted through a smaller surface, resulting in local overheating and significant mechanical stress in SiC chip, which leads to cracking. Comparative analysis of decapsulated samples indicates that cracks and punctures were localized closer to the

source terminals than to drain and gate terminals. However, none distinct correlation between position of bond wire and total amount of lifted bond wires at that position was found. For this purpose, image of SiC chip was divided into 15 areas and cracks or punctures were assigned accordingly. Picture of SiC chip with assigned areas and bond wires labels, and results of visual inspection, are presented in Figs. 40 and 41.



a) b)

Figure 39. Top view of Device Under Test (DUT) $\#1D$ with distinct crack in a SiC die a), and DUT $\#9B$ with puncture burnout of SiC chip b).

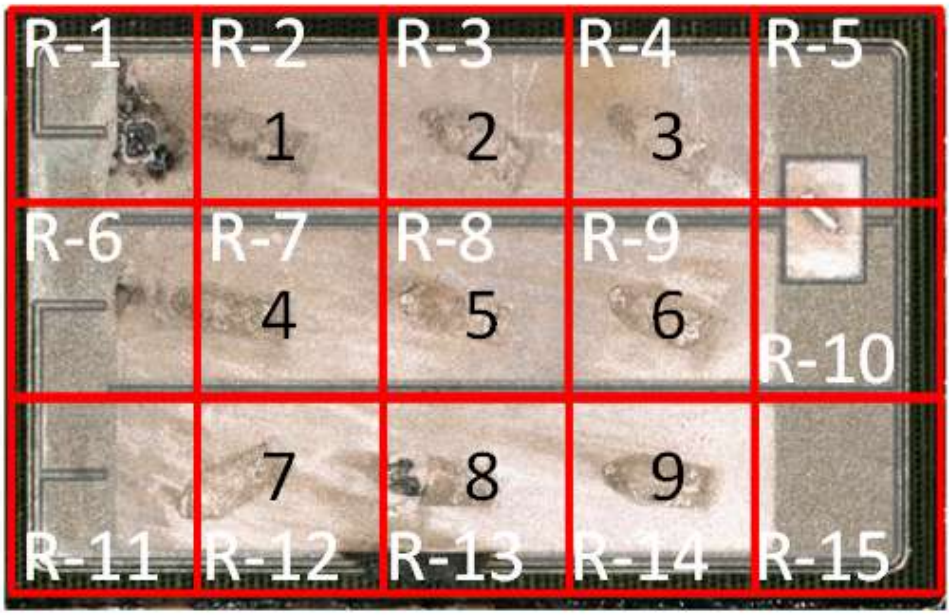


Figure 40. Top view of SiC chip after chemical decapsulation with numered bond wires and quadrants. This diagram was used further for statistical analysis, to confirm whether any of bond wires or parts of SiC chip are more prone to failure than others.

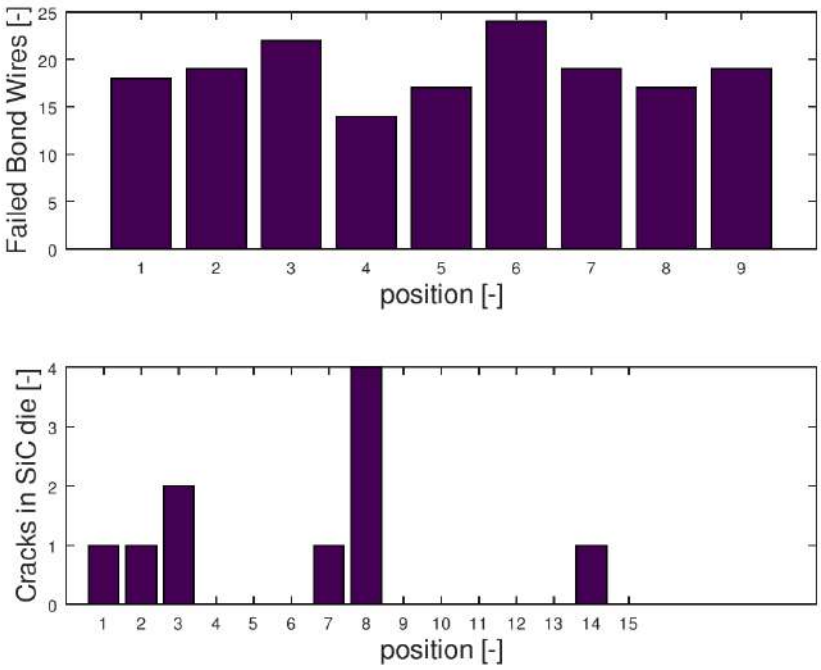


Figure 41. Statistical analysis of failed bond wires and quadrants (see Fig. 40) in which either crack or puncture was found. Results indicates that there is no correlation between position of bond wire and total amount of failed bond wires. There are no clear relationship between amount of cracks and position on SiC chip neither.

Post failure analysis confirms that packaging technology limits lifetime of SiC power MOSFETs in $SOT-227b$ housing. Moreover, presented investigation confirms that failure modes recorded in the ALT are within the scope of *fatigue-like* failure mode definition, which proves that proposed ALT methodology is correct. Thus, test results are found suitable to develop proper reliability model, which could be used to estimate useful lifetime of SiC power semiconductor devices. Identification of proper reliability model and its parameters is presented in the next subsection.

3.3.3 Reliability Model

One of the most recognized mathematical models used in reliability engineering is a Weibull distribution [99], which has been proven as suitable for various failure-modes of semiconductor power devices - from fatigue of solder interconnection [186] to TDDB of gate-oxide layer [187]. Thus, it is expected that Weibull model shall be also suitable

for *fatigue-like* failure modes. To confirm this thesis, a various mathematical models were fitted to failures with the Maximum Likehood Estimation (MLE) algorithm. As depicted in Fig. 42, neither of compared distributions (2- and 3- parameter Lognormal, 1- and 2- parameter Exponential, Logistic, Normal) allowed for significantly better fitting. Moreover, visual inspection and analysis of Anderson-Darling test results suggests that either 2- and 3- parameter Weibull model assures satisfactory projection of recorded data. Thus, the Weibull model was chosen for further investigation.

Typically, the Weibull distribution is described with equation (17), where Probability Density Function (PDF) or $f(x)$ is described with three model parameters: β, η and γ called Shape Parameter, Scale Parameter and Location Parameter respectively.

$$f(t) = (\frac{\beta}{\eta})(\frac{t-\gamma}{\eta})^{\beta-1}(e^{-(\frac{t-\gamma}{\eta})^{\beta}}) \tag{17}$$

Next, the β, η and γ parameters were identified for each distribution. Then, the probability plots were drawn accordingly, as depicted in Fig. 43. As the β is related to failure mode itself, and common failure mode was already confirmed for all samples during post-failure analysis, the common β was assumed for all models. Although models presented in Fig. 43 properly project reliability of SiC MOSFET, there are still far from any useful form. As an example, each of these models is correct only for specific stress level - e.g. junction temperature swing or maximum junction temperature. Thus, the universal model, which could be used in DfR, was developed.

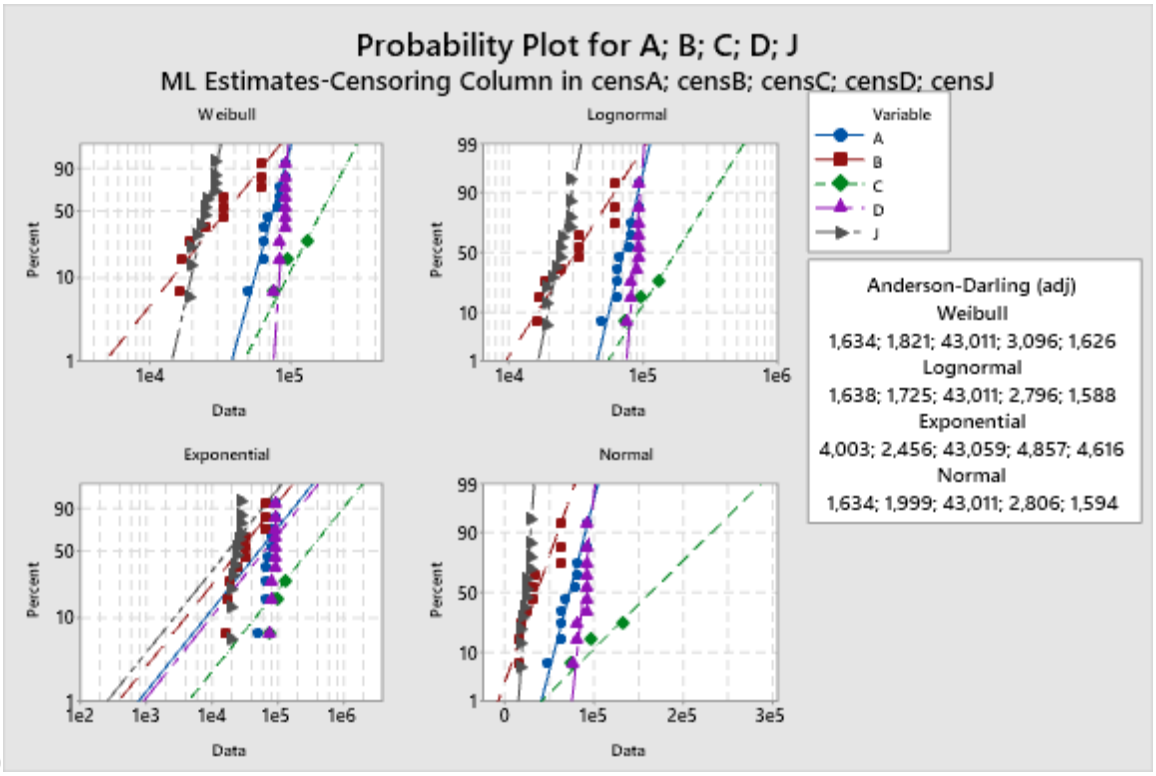
For this purpose, the η had to be modified to form of multivariable function. Either LESIT [188], originally developed for solder connections, or CIPS2008 model [189], originally developed for Si IGBT modules, could be used. Original forms of LESIT model and CIPS2008 model are presented in (18) and (19), respectively.

$$N_f = A \cdot (\Delta T_J)^{\alpha} \cdot exp^{\frac{E_A}{k_B \cdot (T_{MEAN}+273)}} \tag{18}$$

$$N_f = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_J+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{19}$$

These models returns the Mean Useful Lifetime (N_f) expressed in cycles, while parameters A, K, α, β_1 - β_2 are the material constants, E_A is Activation Energy and k_B is Boltzmann

a)



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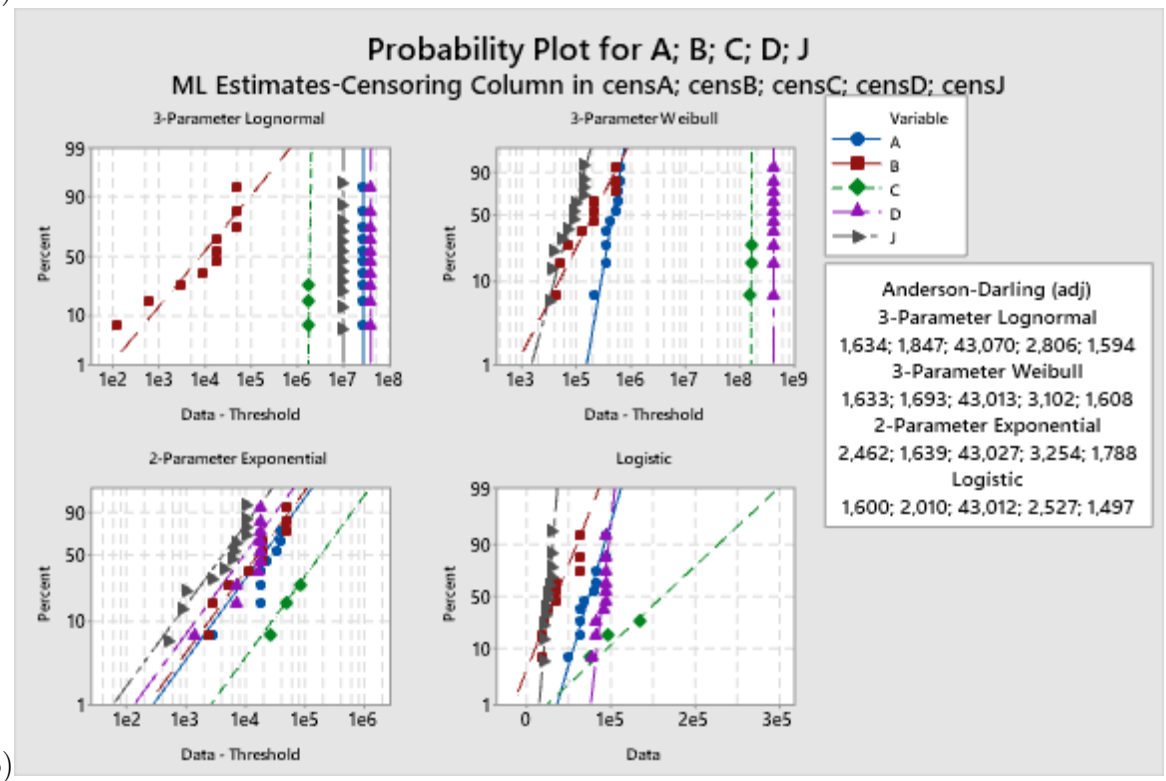
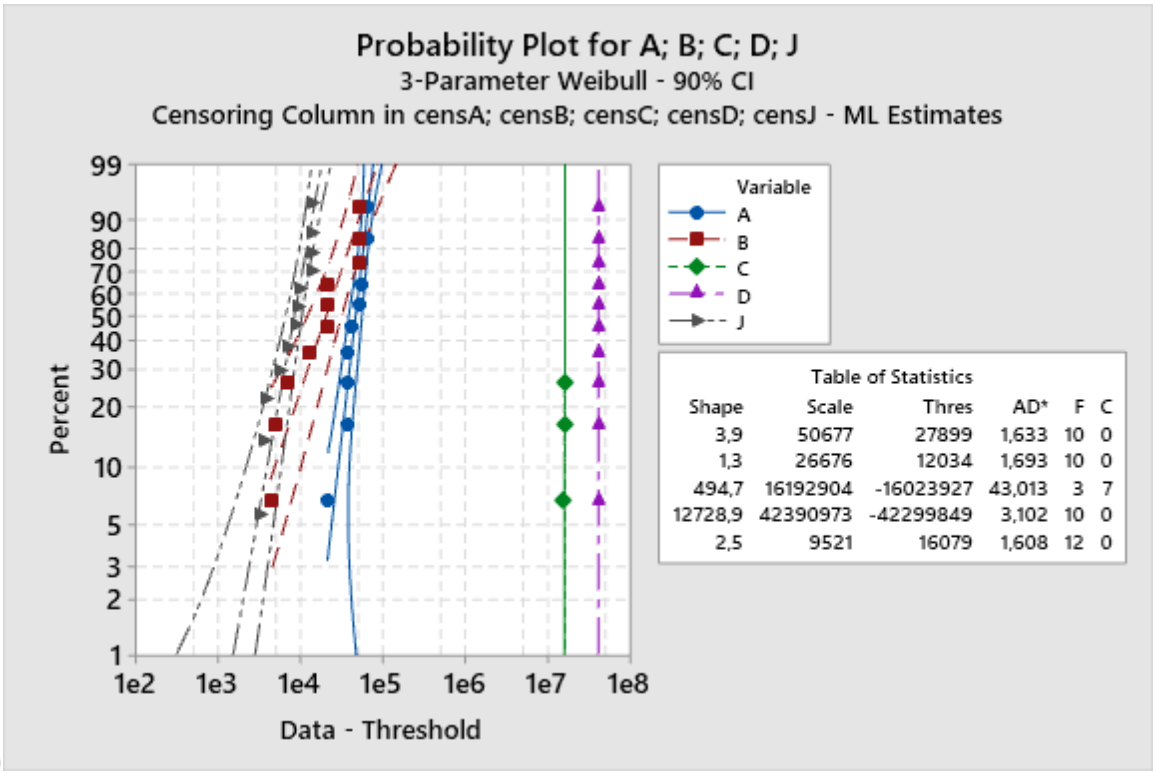


Figure 42. Cross-comparison of various mathematical distributions fitted to the Accelerated Lifetime Test (ALT) results [184].

a)



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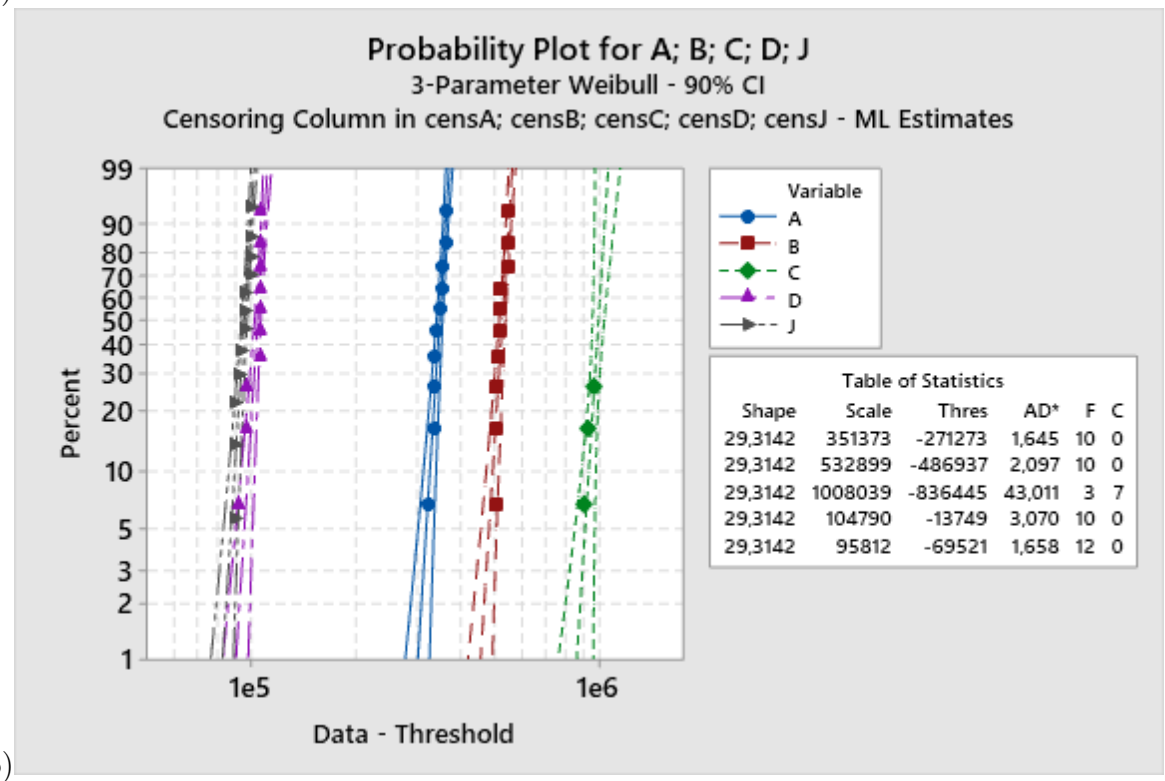


Figure 43. Probability plots prepared for each tested sample set of *SiC* power MOSFET, based on 3-parameter Weibull model asumming separate a) and common b) the Shape Parameter (β) [184].

Constant. In both formulas, ΔT_J, Mean Junction Temperature (T_{MEAN}), and $T_{J_{MAX}}$, are expressed in Celcius. In addition, CIPS2008 model includes also impact of t_{ON}, Current per Wire Bond (I), Chip Blocking Voltage (V) and Diameter of Bonding Wire (D) in useful lifetime calculation.

As it was stated in previous paragraph, either LESIT or CIPS2008 model were originally developed for different applications. Thus, all constant parameters had to be identified based on the ALT test results. As all power cycles were performed with the same t_{ON}, and only one kind of SiC power MOSFET was subjected for ALT, the CIPS2008 model could be simplified into following form (20).

$$N_f = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_{J_{MAX}}+273}} \cdot I^{\beta_3} \tag{20}$$

Therefore, to prepare a universal model, a Weibull model in which the η is a function of stress levels, equations (18) and (20) were used.

$$\eta_1(\Delta T_J, T_{J_{MAX}}) = A \cdot (\Delta T_J)^{\alpha} \cdot exp^{\frac{E_A}{k_B \cdot (T_{J_{MAX}}+273)}} \tag{21}$$

$$\eta_2(\Delta T_J, T_{J_{MAX}}, I_{DS}) = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_{J_{MAX}}+273}} \cdot I_{DS}^{\beta_3} \tag{22}$$

The last remaining parameter in Weibull distribution formula (17) is the *location* parameter. For discussed universal model, it was assumed that failure may occur at any time, resulting in $\gamma = 0$. This allowed to simplify 3-parameter Weibull distribution to it's 2-parameter equivalent (23). This form was used to prepare a universal model, suitable for the purposes of a DfR procedure.

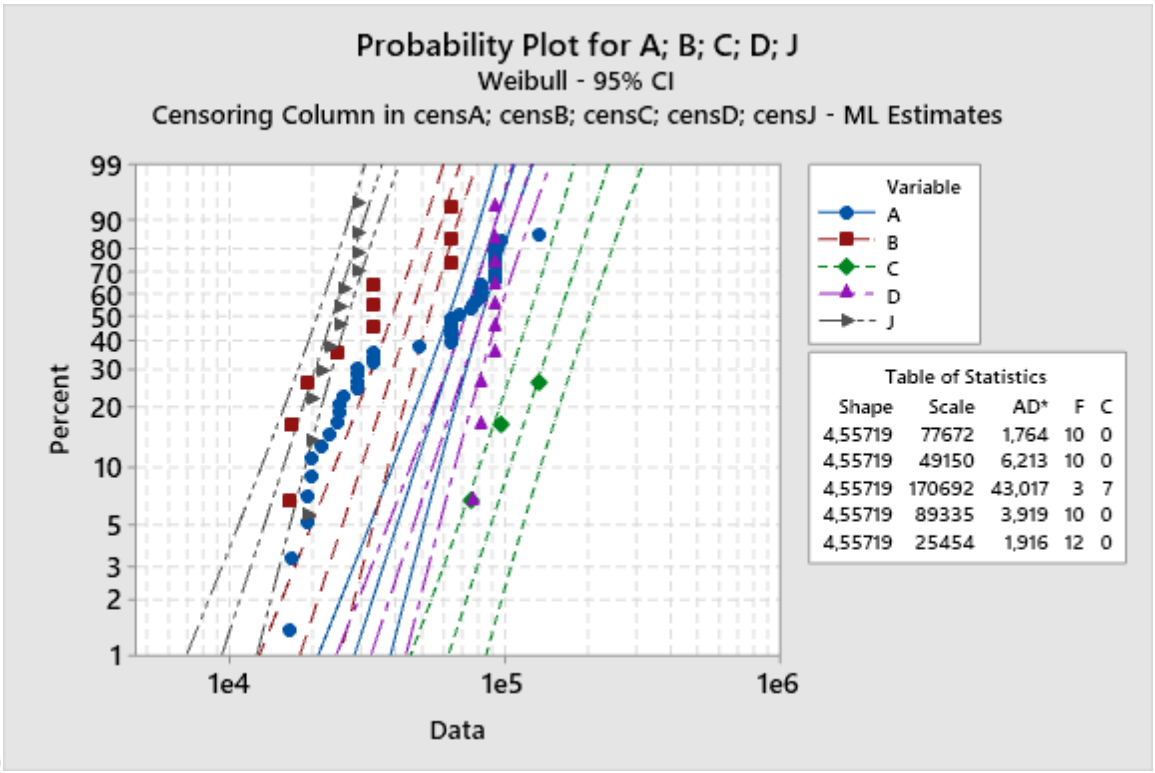
$$f(t) = (\frac{\beta}{\eta})(\frac{t}{\eta})^{\beta-1}(e^{-(\frac{t}{\eta})^{\beta}}) \tag{23}$$

Thus, probability plots depicted in Fig. 43 were replaced with 2-parameter equivalents, as presented in Fig. 44.

To identify material parameters given in Eqs. (21)-(22) a multiple linear regression was performed. The residual plot depicted in Fig. 45a), indicated that:

- there was no correlation between residuals,

a)



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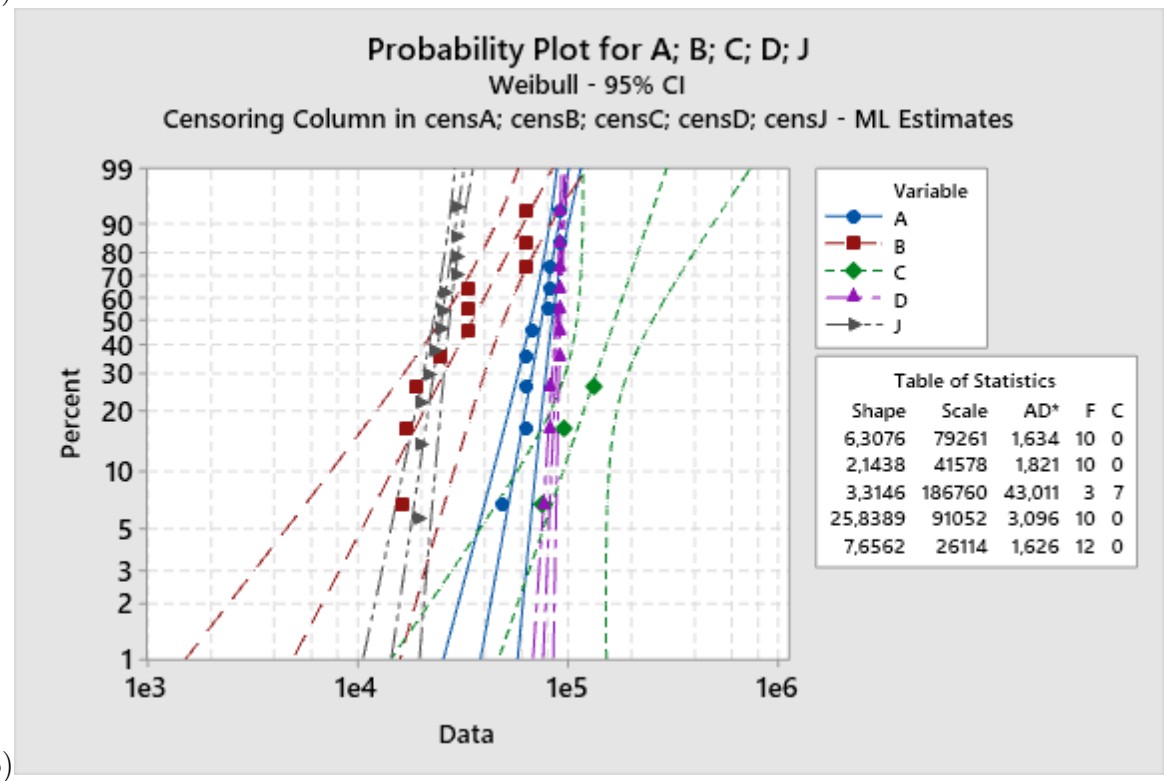


Figure 44. Probability plots prepared for each tested sample set of *SiC* power MOSFET, based on 2-parameter Weibull model assuming separate a) and common b) Shape Parameter (β) [184].

Table 9. Material constants identified for LESIT and CIPS2008 models [184].

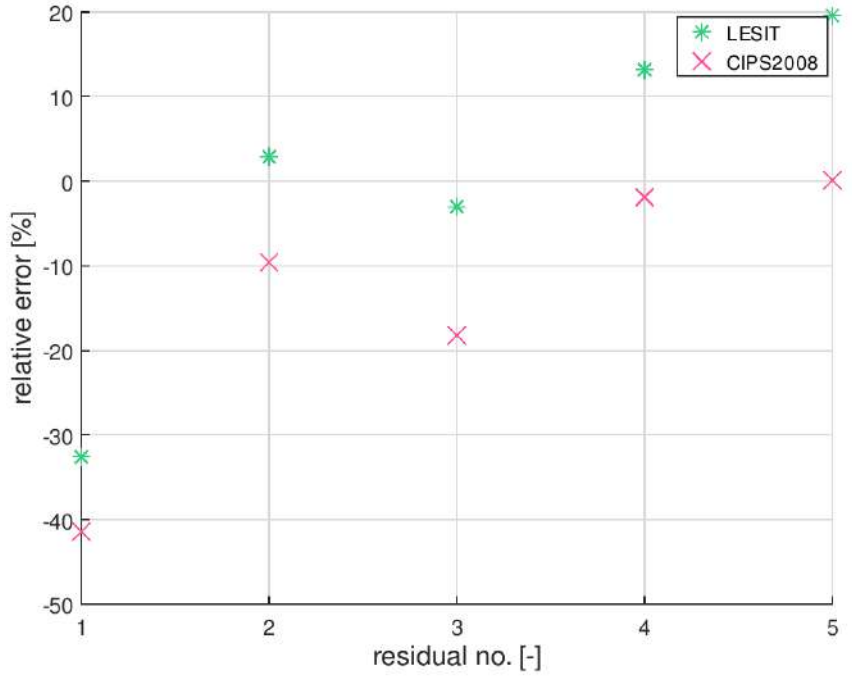
Parameter	$LESIT$	Parameter	$CIPS2008$
A	$1.65e15$	K	$3.37e13$
α	-5.96	β_1	-3.88
k_B	$1.38e-23$	β_2	31.73
E_A	$3.11e-25$	β_3	-0.82

- usage of the LESIT model results in significantly higher estimation error than in the case of CIPS2008 model.

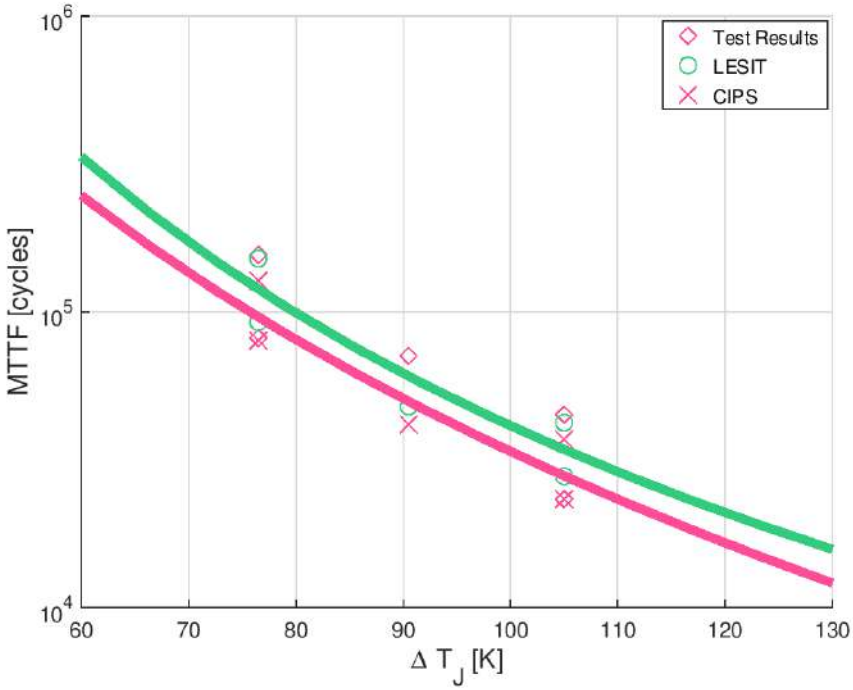
The second conclusion was additionally confirmed when MTTF of SiC power MOSFETs subjected to APC test was compared with developed models. As presented in Fig. 45b) both the LESIT model and the CIPS2008 model offer satisfactory projection of laboratory test results.

Thus, both models were found suitable for reliability modelling of SiC power MOSFET in $SOT-227B$ housing. However, a simplified form of CIPS2008 equation was chosen for further evaluation of the universal reliability model. This decision was caused by simple fact that even simplified form of CIP2008 model cover higher amout of stress factors. The identified values of material constants and activation energy, corresponding to Eqs. (21) - (22) are listed in Tab. 9.

At last, the MTTF curves for different ΔT_J and I_{DS} values were identified. Both Fig. 46a) and closer analysis of β_1 and β_3 parameters suggests that ΔT_J has significantly higher impact on power MOSFET reliability than the I_{DS}. Furthermore, the PDF for SiC power MOSFETs subjected to various operating conditions were prepared with presented universal model (see Fig. 46b)). Based on such PDFs it is possible to calculate how failure rate changes over the time, or what is power MOSFET useful lifetime defined as mean value (same as MTTF), or so-called *BX life* - the time at which $X\%$ of MOSFETs will fail. These data may be further used in DfR procedure to estimate either railure rate or useful lifetime of high performance power converter.

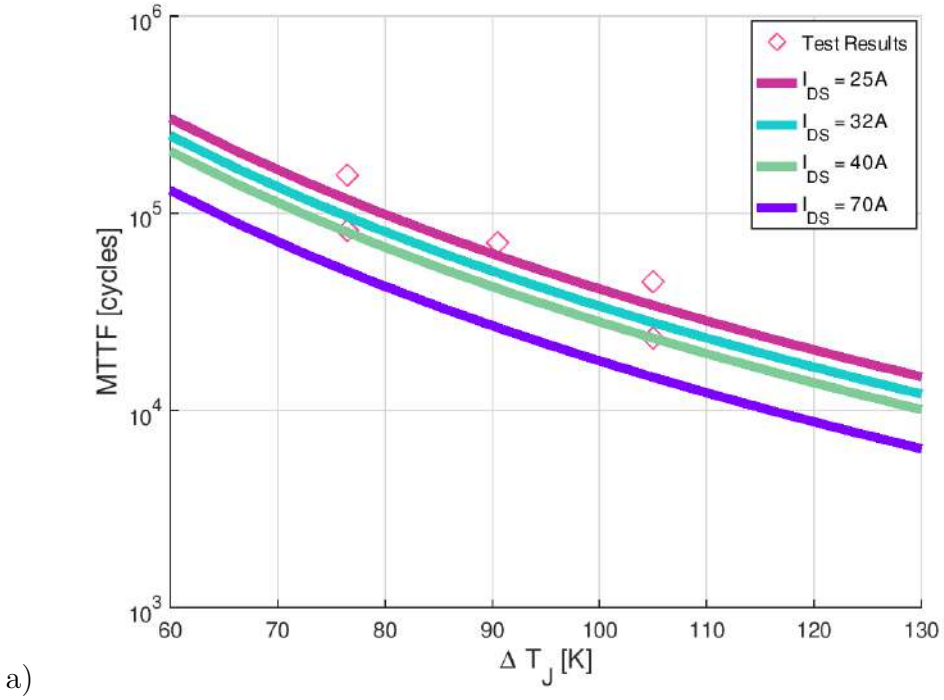


a)

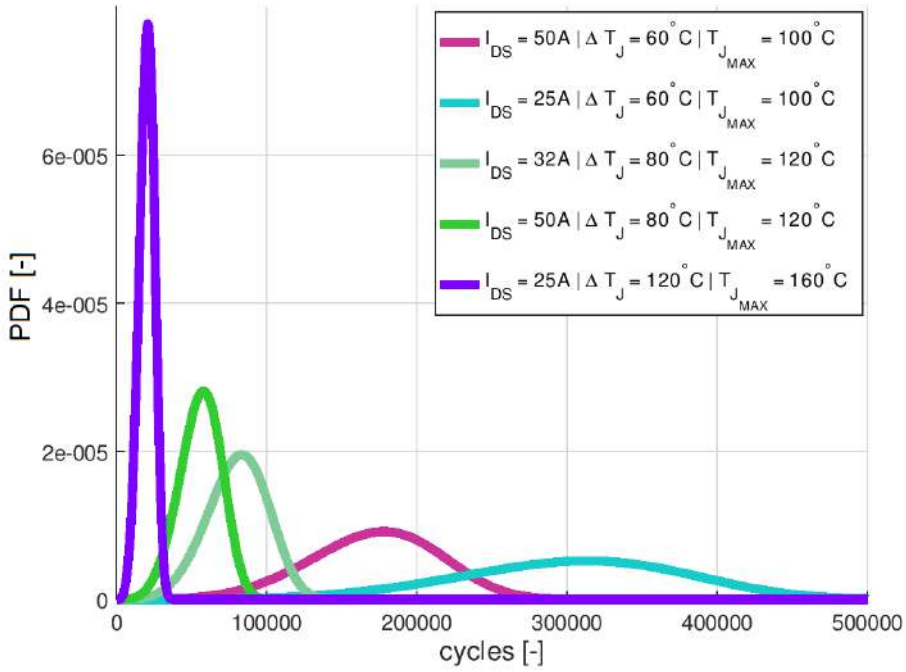


b)

Figure 45. Residual plot for Weibull distribution Scale Parameter (η) estimators, based on LESIT and CIPS2008 models a), comparison of test results with MTTF for *SiC* power MOSFET estimated based on Weibull-LESIT model and Weibull-CIPS model b) [184].



a)



b)

Figure 46. Mean Time To Failure (MTTF) estimation for *SiC* power MOSFETs subjected to power cycling at various operating conditions. The ambient temperature assumed in analysis is $40°C$ a), probability density functions derived for *SiC* power MOSFETs subjected to power cycling at various operating conditions b) [184].

3.4 Conclusions

In this chapter, a methodology for conducting a Power Cycling (PC) test on SiC power MOSFETs in $SOT-227B$ housing is presented. The PC test was chosen to perform the Accelerated Lifetime Test (ALT), for the identification of reliability model parameters for SiC power MOSFET in $SOT-227B$ housing. Presented methodology was proven as valid for performing a ALT test optimized for *fatigue-like* failure mode, thanks to the extensive post-failure analysis (X-RAY imaging, Confocal Scanning Acoustic Microscopy (CSAM) and decapsulation). Although reliability modelling and PC of SiC devices were investigated by various researchers, the previous papers were focused on multichip IGBT or MOSFET modules [160, 161] and discrete devices in $TO-220$ or $TO-247$ housing [147, 159]. The industry-grade $SOT-227B$ housing, for high power semiconductor devices, has not been investigated yet.

Beside testing strategy itself, technical aspects of the test bench for the ALT of SiC power MOSFETs in $SOT-227B$ housing are presented. In contrast to the setups presented by other researchers, presented test bench allows to perform a ALT in industry-friendly manner - with 120 Devices Under Test (DUTs) at once. Designed gate voltage controller circuit was proven to fulfill all key requirements:

- good thermal stability,
- good accuracy of Drain-Source Voltage (V_{DS}),
- low Junction Temperature Dispersion Between Neighboring Samples ($T_{J_{(n)-(n+1)}}$).

At last, designed failure detection algorithm for ALT allowed to mitigate effects of failure of power MOSFET, and protected SiC chip from complete destruction, which enabled the post-failure analysis of DUTs. This procedure allowed not only, to understand in details Physics of Failure (PoF) of SiC power MOSFET subjected to the ALT, but also compare effectiveness of various examination techniques.

Presented reliability model for SiC power MOSFETs in $SOT-227B$ housing, fits well to the obtained data. Moreover, proposed approach of combining a Weibull distribution with a CIPS2008 model, allows to obtain the PDF for various operating conditions. Thus, it is found suitable for purposes of DfR procedure.

Future research on lifetime modelling of SiC power MOSFET in $SOT-227B$ housing may address following issues:

- Low Amplitude of Junction Temperature Swing (ΔT_J) - below $40°C$.

  As presented in [190], strong experimental evidence suggests that the degradation process accelerates toward EoL. Therefore, it is possible to define *linear* and *non-linear* ageing phases for thermomechanical failure modes. Although low ΔT_J temperature swings do not significantly contribute to lifetime consumption during the linear stage of the ageing process, this impact is no longer negligible whenever solder crack initiates or the bond-wire starts to lift-off and the power semiconductor reaches its lifetime non-linear stage. In addition, in the linear ageing phase of the power semiconductor, some of the materials used for manufacturing remain in the elastic region. When these materials reach the plastic region, their hysteresis stress-strain plots are shifted, which results in their deformation after subjecting the power semiconductor to thermomechanical stress. Therefore, the power semiconductor reaches the non-linear ageing phase. In this case, it is expected that a reliability model extracted from ALT results may introduce an underestimation of the power MOSFET useful lifetime for low temperature swing.

- Different t_{ON} and t_{OFF} ratio and duration of the power cycle or different power profile.

  As mentioned in section 3.1.1, the heating profile has a significant impact on the test results due to the change in the leading failure mode. In this case, the reliability model would only be correct for very specific heating profiles - the same as used during ALT. This leads to the following questions: How to extrapolate lifetime estimation for different heating profiles (e.g. different duty cycle and period)? What would the lifetime estimation error be if this relationship between the duty cycle of the heating profile and power MOSFET reliability were ignored?

- Switching losses instead of conduction losses.

  In typical applications (e.g. AC-DC converter, DC-DC converter) the power

MOSFET is subjected to high switching losses and a small part of conduction losses, which might also impact on lifetime estimation accuracy.

Chapter 4

Case Study analysis for proposed DfR procedure

The last chapter of this thesis is focused on practical examples of proposed DfR procedure. However, products from TRUMPF's portfolio could not be used for this purpose, as close analysis of e.g. electrical models or schematics would reveal company know-how and intellectual property. Thus, the alternate approach was proposed. To present first five stages of modified DfR procedure (from *Technical Specification* stage to *Proof of Concept* phase), a Power Electronic Building Block (PEBB) for a modular power converter, based on the Wide-Bandgap (WBG) power semiconductor devices, was designed. This research is further discussed in [110].

4.1 Reliability Oriented Design of Power Electronic Building Block module

Previous research suggests that following topology are suitable as power building blocks for large power conversion systems:

- H-bridge,
- Dual Active Bridge (DAB),
- two-level single- or three-phase leg inverter,
- three-level neutral-point clamped inverter,
- T-type converter,

- synchronous resonant quasi-Z-source DC-DC converter.

However, a closer analysis of the above-mentioned power converters shows that all of them can be successfully represented as the series-parallel connection of multiple half-bridge modules. Therefore, to assure high *configurability* of discussed modular power converter, the basic power electronic building block used in it has to be a half-bridge topology, similar to the concept investigated in [191]. The PEBB concept itself is very interesting for the reliability-oriented designs, thanks to high element re-usage, which greatly simplifies the reliability estimation. As depicted in Fig. 47, even complex design can be represented as set of functional modules, with properly defined failure rates.

a)

b)

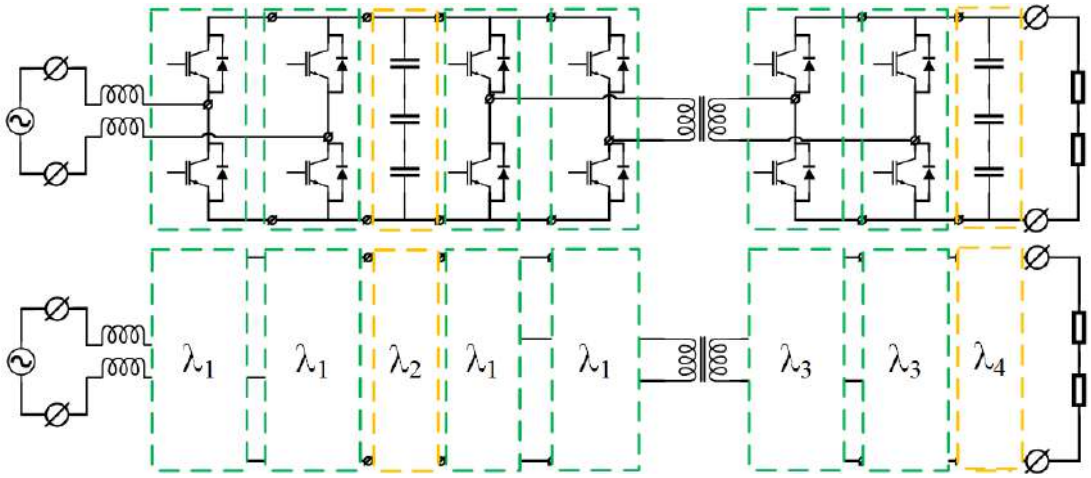


Figure 47. Graphical representation of example PEBB-based power converter and corresponding reliability block diagram [110].

The first step of DfR procedure - the boundary conditions are defined as a set of functional requirements (e.g. describing power converter behavior or work modes) and operating conditions. As an example, functional requirements for PEBB-based converter and PEBB module could be defined as follows:

- PEBB module has to be air-cooled.
- PEBB-based power converter has to assure output voltage linear regulation.
- PEBB-based demonstration power converter has to be the Buck converter.
- Reliability goal is MTBF no less than 5 years.
- PEBB module has to support the Reliability-Oriented Control (ROC) algorithm.
- Etc.

In contrast, a operating conditions are measurable, countable and well-defined, as presented in following examples:

- Target application - buck converter.
- Target load - 30 Ω
- Output Voltage - 200 V_{RMS}
- Ambient temperature - 30°C
- Switching frequency - 100 kHz
- Input voltage - 400 V
- Relative humidity - $\geq 85\%$
- Mission profile is continuous power cycling - $t_{ON} = 1\ s$, $t_{ON} = 1\ s$, $P = P_{NOMINAL}$
- Etc.

In presented example, the topology of PEBB-based demonstration power converter was defined *a priori*, thus the simulation stage was focused only on selection of the critical components, and the rough stress level estimation. The detailed discussion over active component selection and simulation study was presented in [192], and was initiated with the benchmark analysis of WBG devices for low-power applications. At first, the $600-650\ [V]$ components were found as the optimum compromise between keeping proper voltage derating for 400 $[V]$ PEBB module and cost efficiency of demonstration PEBB-based power converter. Then, state-of-the-art WBG components in $TO-247$ housing, listed in Tab. 10, were chosen for further evaluation. Next, selected WBG devices were subjected to comparative analysis, focused on fundamental electrical parameters, e.g.: $R_{DS_{ON}}$, rated I_{DS}, $Z_{TH_{JC}}$, maximum allowed V_{GS}, Total Gate Charge (Q_G). To complete the comparative study, switching and conduction losses were estimated analytically for each transistor, and depicted side-by-side with electrical parameters in Fig. 48. Based on this analysis, $TP65H035WS$ (T5), $TP65H035G4WS$ (T6) GaN cascodes and $UF3C065040K3S$ (T1) SiC cascode were considered as most solutions for discussed demonstration PEBB-module. The PEBB-module discussed in this case study was designed with the $UF3C065040K3S$ (T1) SiC cascode.

Table 10. Proposal of $600-650\ V$ Wide-Bandgap (WBG) power semiconductor devices suitable for demonstration modular power converter based on Power Electronic Building Block (PEBB) concept [110].

	Part Number	Label	Current Rating	$R_{DS_{ON}}$
[-]	[-]	[-]	$[A]$	$[m\Omega]$
SiC	$UF3C065040K3S$	$T1$	54	42
	$IMW65R027M1HXKSA1$	$T2$	47	27
	$SCT3060ALGC11$	$T3$	39	60
	$SCT3030ALHRC11$	$T4$	70	30
GaN	$TP65H035WS$	$T5$	46.5	41
	$TP65H035G4WS$	$T6$	46.5	41
	$TP65H070LDG$	$T7$	25	85
	$IGT60R070D1ATMA1$	$T8$	31	70

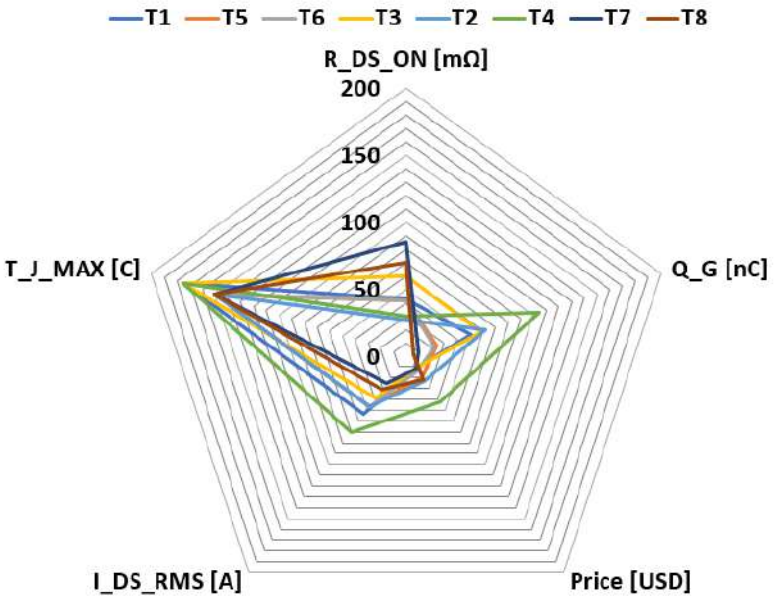


Figure 48. The radar chart with graphical comparison of key parameters of Wide-Bandgap (WBG) power semiconductor devices.

Table 11. Stress levels for semiconductor power devices used in PEBB-based buck converter.

Stressor	unit	T1sym	T2sym
$V_{DS_{PEAK}}$	$[V]$	404	399
$V_{DS_{RMS}}$	$[V]$	286	282
$I_{DS_{PEAK}}$	$[A]$	10.9	10.97
$I_{DS_{RMS}}$	$[A]$	4.98	-4.99
ΔT_J	$[°C]$	29.3	37.9
$T_{J_{MAX}}$	$[°C]$	54.3	62.9

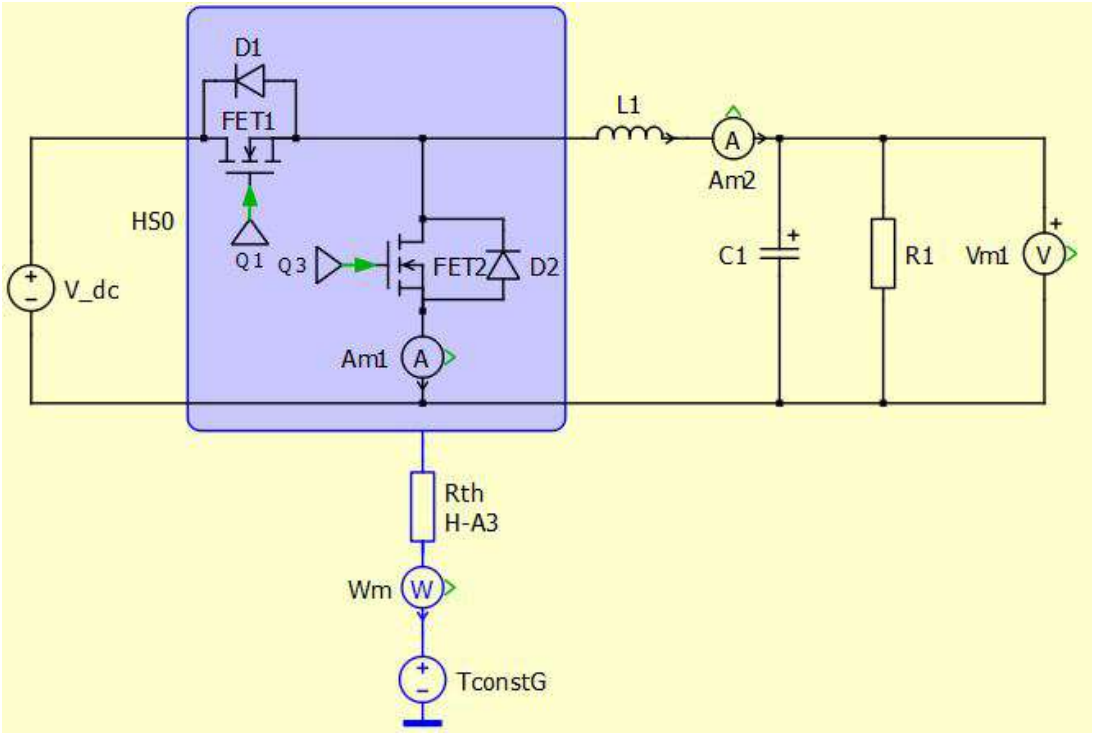
Afterwards, it was confirmed if proposed topology allows to fulfill functional requirements. The PLECS model used for this purpose is presented in Fig. 49a), while the detailed list of stress level for active components is presented in Tab. 11. To estimate transients values, corresponding simulation was performed in SPICE environment, as depicted in Fig. 49b). The detailed discussion over active component selection and simulation study were presented in [192].

Next stage of the proposed DfR procedure are component- and system-level lifetime estimation, performed in parallel to electrical design. In the presented example of the PEBB module, there are only two types of critical components:

- WBG power devices (FET1, FET2),
- Output capacitor (C1).

However, it was impossible to use reliability model discussed in 3.3.3 in reliability assessment of PEBB-based demonstration power converter, as PEBB-module was designed with WBG-devices in $TO-247$ housing. Due to significant difference in construction between $TO-247$ and $SOT-227B$ housing, such approach would be simply erroneous. Thus, the reliability evaluation of the PEBB-based buck converter discussed in this paper may be subjected to rather significant error, as it is based on test results presented in research papers and publicly available materials. However, the main goal of presented case study is rather explanation *how* reliability assessment or other key steps of DfR procedure should be performed, than *exact* reliability estimation. Thus, in the case of presented PEBB-

a)



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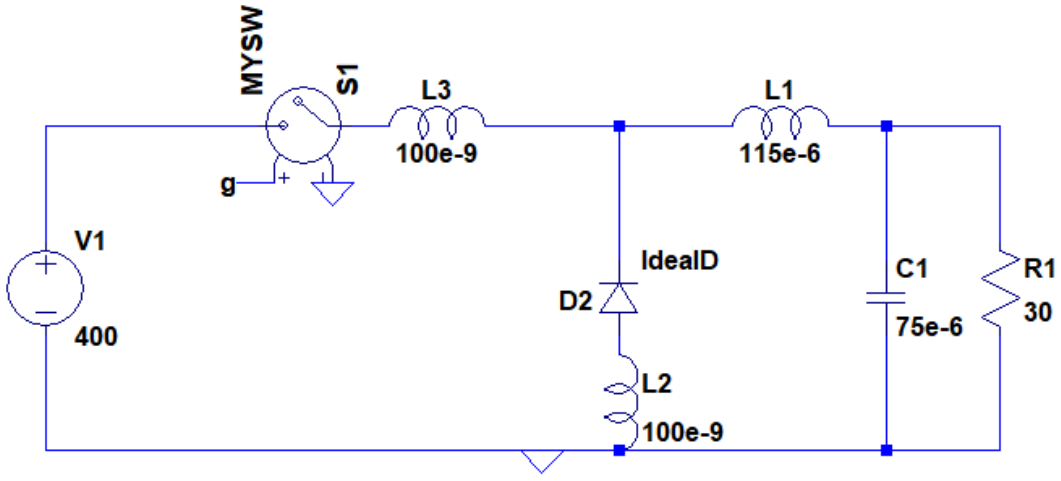

Figure 49. Electrical model used for steady-state stress levels estimation [110].

based demonstration power converter, the absolute accuracy of reliability predictions is not relevant.

As presented in 2.1, the UL of discrete SiC power devices is mostly limited by durability of the bond-wires, although other *fatigue-like* failure modes also play important role. As discussed in 3.3.3, the reliability models suitable for analysis of such failure mechanisms are the LESIT model and the CIPS2008 model. However, the CIPS2008 model was originally designed for IGBT modules. Thus, for UL estimation the LESIT model presented in [129] was used. This particular model was found more suitable than the CIPS2008, as it was identified for GaN HEMT devices in $TO-220$ housing. $TO-220$ housing is very close to the $TO-247$ housing, of SiC power MOSFETs used in the demonstration power converter. Moreover, the bond wire fatigue is typical package-related failure mechanisms, which is rather affected by the packaging technology, than the type of semiconductor chip. Thus, this particular LESIT model was found as the most suitable for UL estimation of SiC cascode. Next, the estimated stress level values were substituted to Eq. (24) to assess the number of cycles before failure. Then, the working time expressed in years was calculated, assuming 24 hour per 7 days a week operation with earlier mentioned mission profile - power cycling $t_{ON} = 1\ s$, $t_{OFF} = 1\ s$. Mission profile was depicted in Fig. 50. The UL, represented in a number of power cycles and years of work, is presented in Tab. 12.

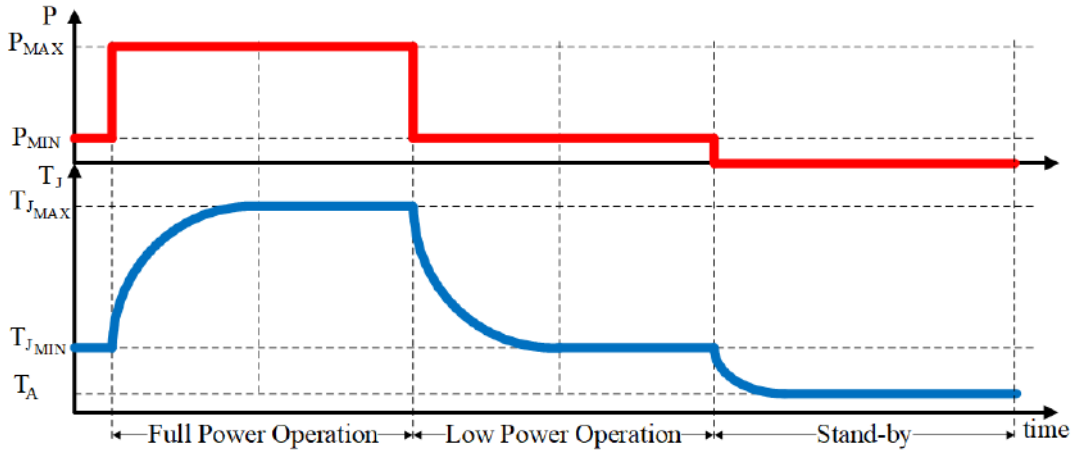

Figure 50. Example mission profile of PEBB-based buck converter [110].

$$N_f = 6 \cdot 10^{20} \cdot \Delta T_J^{-8.112} \tag{24}$$

Table 12. Estimated useful lifetime of Wide-Bandgap (WBG) power semiconductor devices.

	FET1	FET2
Cycles to failure $[10^9]$	$757e6$	$93.8e6$
Working time $[years]$	~ 48	~ 6

As presented in 2.2, the dominant failure mode of SiC power devices in their UL are Single Event Effects (SEE). Thus, to estimate the Failure Rate (FR), the reliability model presented in [124] was used. Based on the maximum V_{DS}, and referenced model, failure rates were calculated as follows:

- Failure Rate for transistor T1: 12.5 $\frac{failures}{10^9\ hours}$,
- Failure Rate for transistor T2: 12.5 $\frac{failures}{10^9\ hours}$.

The second major critical component of the presented PEBB-based buck converter are foil capacitors used for output filter, whose main stressors are: voltage, temperature, and humidity [193]. For purposes of the case study analysis, it was assumed that foil capacitors do not degrade or wear out, thus they have a constant FR. Such assumption could not be done, if demonstration power converter would operate in tropic or humid environment, due to high risk of humidity-induced degradation of failure. However, boundary conditions listed in previous paragraphs clearly defined low relative humidity for both storage and operation. Next, the target FR was estimated based on the base failure rate (λ_0) and proper temperature and voltage correction factors (π_T, π_V), as presented in Eq. (3) in Chapter 2.

$$\lambda = \lambda_0 \cdot \pi_T \cdot \pi_V = 2 \cdot 1 \cdot 2 = 4 \tag{25}$$

Thus, stress levels estimated during simulation study and data given by foil capacitor manufacturer [112], the failure rate of output filter was denoted as 4 $\frac{failures}{10^9\ hours}$ per capacitor.

The next step of proposed DfR procedure is module- and system-level reliability assessment. Of course, presented PEBB-based power converter consists many more critical

components than only WBG power semiconductor devices or foil capacitors. However, they are not essential for the tutorial purposes of presented case study analysis, and therefore they are not further discussed in this reliability assessment. In general, FR of integrated circuits, small-signal semiconductor devices, resistors, connectors, etc. can be takes from datasheet or estimated based on any suitable standard - e.g.:

- Military Handbook: Reliability Prediction of Electronic Equipment MIL-217F-HDBK [194],
- European Reliability Prediction Standard IEC-62380 [195],
- European Reliability Prediction Standard IEC-61709 [196],
- FIDES Reliability Methodology for Electronic Systems Guideline [197],
- Telcordia SR-332 Reliability Prediction Procedure for Electronic Equipment [198],
- Siemens SN 29500 Electronic Reliability Prediction standard,
- etc.

Then, the module-level reliability assessment can be done with proper Reliability Block Diagram (RBD), Markov Diagram (MD) or Fault-Tree Analysis (FTA). If any component failure leads to module's malfunction, Module Failure Rate (λ_{MODULE}) can be represented as sum of Failure Rates of critical components (λ_n) , as presented in Eq. (26).

$$\lambda_{MODULE} = \sum_{n=1}^{k} \lambda_n \tag{26}$$

Thus, if PEBB module consists of only 2 critical components (transistors $T1$ and $T2$, 12.5 $\frac{failures}{10^9\ hours}$ each), and DC-link consists of 6 foil capacitors (4 $\frac{failures}{10^9\ hours}$ each), $\lambda(t)$ for these modules will be 25 $\frac{failures}{10^9\ hours}$ and 24 $\frac{failures}{10^9\ hours}$, accordingly.

System-level reliability assessment is performed in the same way as the module-level reliability assessment. Therefore, the total failure rate of PEBB-based buck converter was found 49 $\frac{failures}{10^9\ hours}$, which corresponds to MTBF 20.4 million hours. Based on the estimated useful lifetime, such failure rate should be correct for 5.9 years of operation (see Tab. 12). Thus, it is expected that the reliability goal shall be fulfilled.

Afterwards, a PoC was released and tested. As stated in section 2.2, the main goals of *Proof of Concept* phase in modified DfR procedure are:

- verification if all functional requirements are fulfilled,
- detection and remove of most of design flaws,
- confirmation if stress levels are not higher, than values used for reliability estimation.

Thus, the test routines shall be properly designed to thoroughly evaluate each desired functionality. As an example, to verify proper support of the ROC algorithm, both range of linear regulation and step response of V_{GS} control circuit had to be checked up. The ROC algorithm itself was described in [110], and will not be further discussed in this thesis as irrelevant to the presented case study analysis. As depicted in Figs. 51 and 52, tests confirmed satisfactory accuracy of V_{GS} linear regulation, however the step response showed rather low dynamics of electrical circuit. Nevertheless, this functional requirement was confirmed as fulfilled.

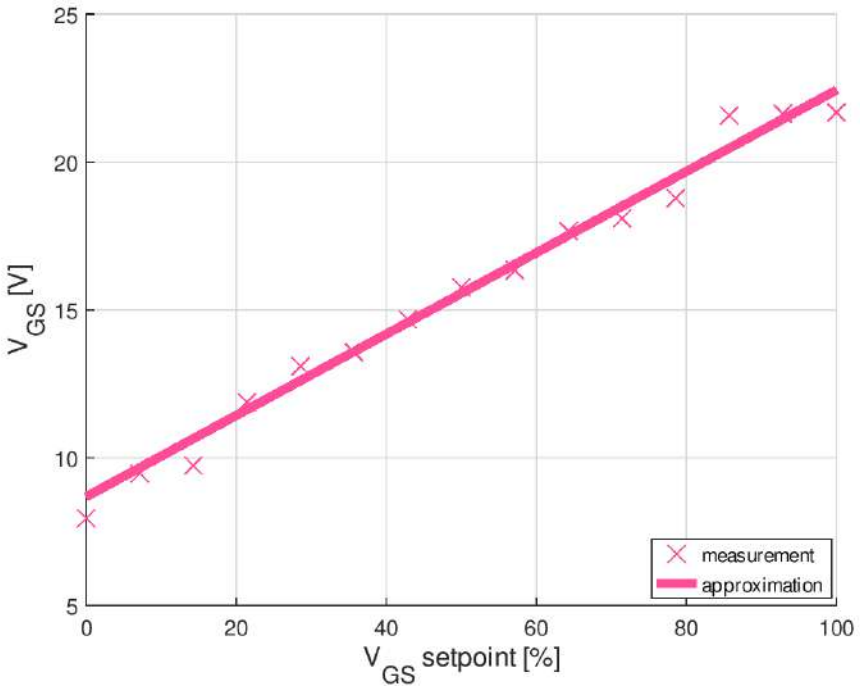

Figure 51. Accuracy and range of V_{GS} controller circuit, which enables Reliability-Oriented Control (ROC) algorithm [110].

Afterwards, the start-up of PEBB-based buck converter was initiated. The test routine designed for this purpose consists of operation for multiple ranges of input/output voltages, switching frequencies, and load conditions. Although the device was designed for

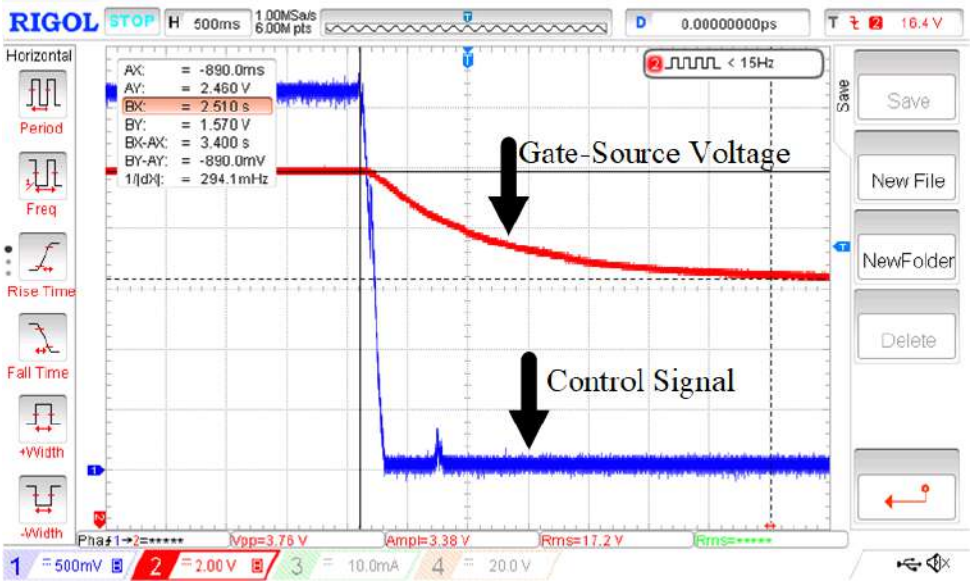

Figure 52. Step response of V_{GS} controller for $V_{GS} = 17.2\ V$ and idle operation [110].

specific operating conditions, the test routine covered a far further range to increase stress levels and visualize any design flaws. As an example, increasing the switching frequency to 200 kHz allowed to highlight the high-frequency oscillations present in the V_{GS} signal, as depicted in Fig. 53a). As it was stated before, such voltage overstress may accelerate the gate oxide degradation, resulting in fatal failure of WBG power semiconductor device. Thus, the following design flaws were identified based on these and other test results:

- a suboptimal design of a commutation loop in a half-bridge module,
- a suboptimal design of gate circuit, which increased a Gate-Drain Parasitic Capacitance (C_{GD}).

To get rid of these design flaws, the PEBB-module was immediately re-designed. It is expected that in typical short TTM projects, time pressure will allow designers to prepare an only single PoC. However, in the case of the presented PEBB-based buck converter, the tutorial effort and proper demonstration of the modified DfR procedure are far more important than the time spent on its development. Thus, these design flaws could be eliminated before reaching the *reliability growth* stage. As presented in Fig. 54, optimization of PCB design allowed to reduce both parasitic commutation loop inductance and C_{GD}. To be more specific, the drain plane was moved away from the driver circuit

and the gate-source terminals. Moreover, few countermeasures were taken to reduce the stray inductance of the commutation loop. Firstly, both output terminals and power MOSFETs were put closer to each other, to decrease the total length of a copper plane from positive to negative terminal. The width of copper planes was also increased. At last, a few DC-link foil capacitors were replaced with ceramic ones. This resulted in far less ringing of either V_{GS} or V_{DS} voltage, as depicted in 53b).

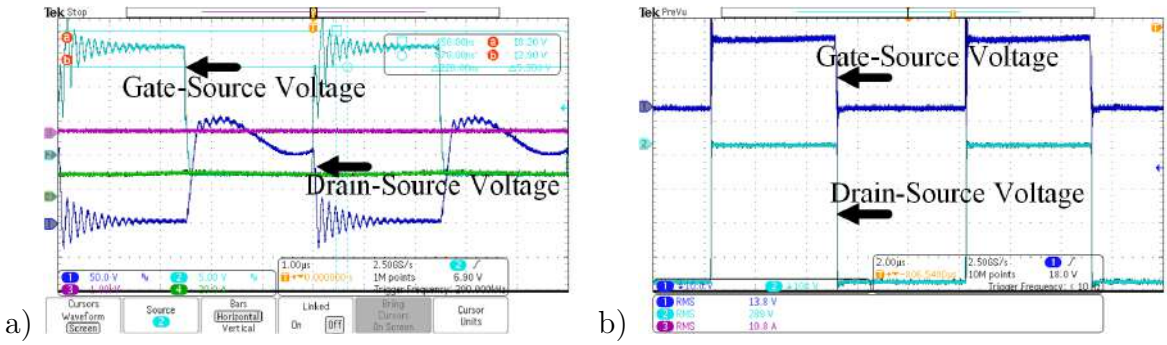

Figure 53. V_{DS} and V_{GS} for initial Proof of Concept (PoC), presented in channel 1 and 2 respectively [110].

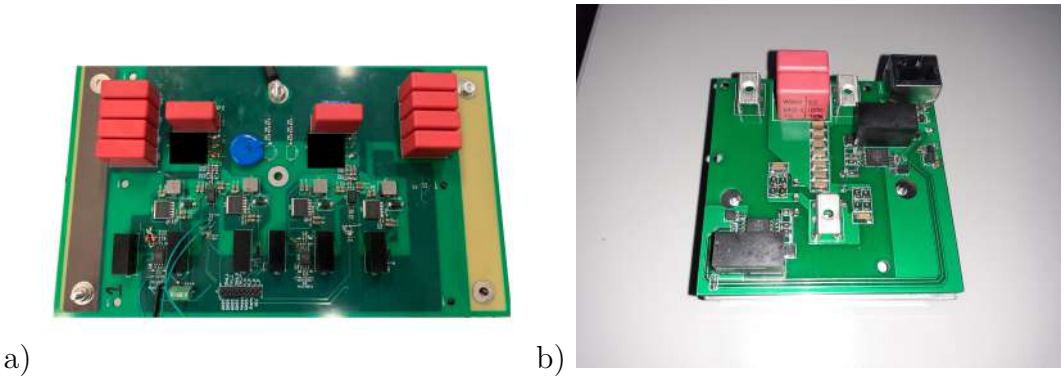

Figure 54. Photography of original Physics of Failure (PoF) of Power Electronic Building Block (PEBB) module a), and photography of PEBB module with minimized commutation loop b) [110].

The cross-comparison of real stress levels and initially estimated values are presented in Tab. 13. Closer analysis showed that stressors were slightly underestimated, however it had no major impact on the estimated failure rate. However, thus to the higher amplitude of junction temperature swing than expected, the useful lifetime of $T2$ power MOSFET was reduced to $\sim 18.8e6$ cycles, which corresponds to ~ 1.2 years of operation. Thus, the

Table 13. Cross comparison of estimated and real stress levels for semiconductor devices in PEBB-based buck converter.

Stressor	unit	T1sym	T2sym	T1real	T2real
$V_{DS_{PEAK}}$	$[V]$	404	399	465	405
$V_{DS_{RMS}}$	$[V]$	286	282	289	285
$I_{DS_{PEAK}}$	$[A]$	10.9	10.97	10.6	10.62
$I_{DS_{RMS}}$	$[A]$	4.98	4.99	5.44	5.4
ΔT_J	$[°C]$	29.3	37.9	34.5	46.2
$T_{J_{MAX}}$	$[°C]$	54.3	62.9	59.5	71.2

reliability goals had not been confirmed, which indicates that the PEBB module requires optimization.

The next steps - *reliability growth* and *reliability demonstration* were not in the scope of presented case study, thus they are not further discussed in this section. As laboratory testing defined for these steps is extremely time-consuming and costly, due to highly invasive nature of stress tests, they are meant only for proven designs. Unfortunately, presentation of test procedures, results or reports prepared for TRUMPF's products was not possible, as it would reveal company know-how and intellectual property. Thus, neither *reliability growth* or *reliability demonstration* was not described with dedicated case study. The last step of proposed DfR procedure is the *reliability maintenance*, for which a practical example is described in the next section.

4.2 Reliability Maintenance - the obsolescence management

As it was described in section 2.3, the main purpose of the *reliability maintenance* procedure is to ensure that reliability goals will be always fulfilled for mass produced power supplies. Thus, in this step the reliability engineering partially overlaps with the quality control and assurance. One of the biggest challenges related to the *reliability maintenance* is the obsolescence management. Every HPPS is an extremely complex system, which consists of many components - from low voltage analog and digital electronics (e.g. drivers,

optocouplers, operational amplifiers), through power electronic semiconductor devices, up to passive components (e.g. foil/electrolytic/ceramic capacitors, inductors). Each of these components has its lifecycle, and at a certain point becomes obsolete, which brings up the question of *how* to ensure that the new counterpart will not negatively affect the reliability of the whole HPPS. This can be done with thorough analytical study, simulation study or with proper Reliability-Oriented Comparative Test (ROCT). Such a test is presented in this case study analysis.

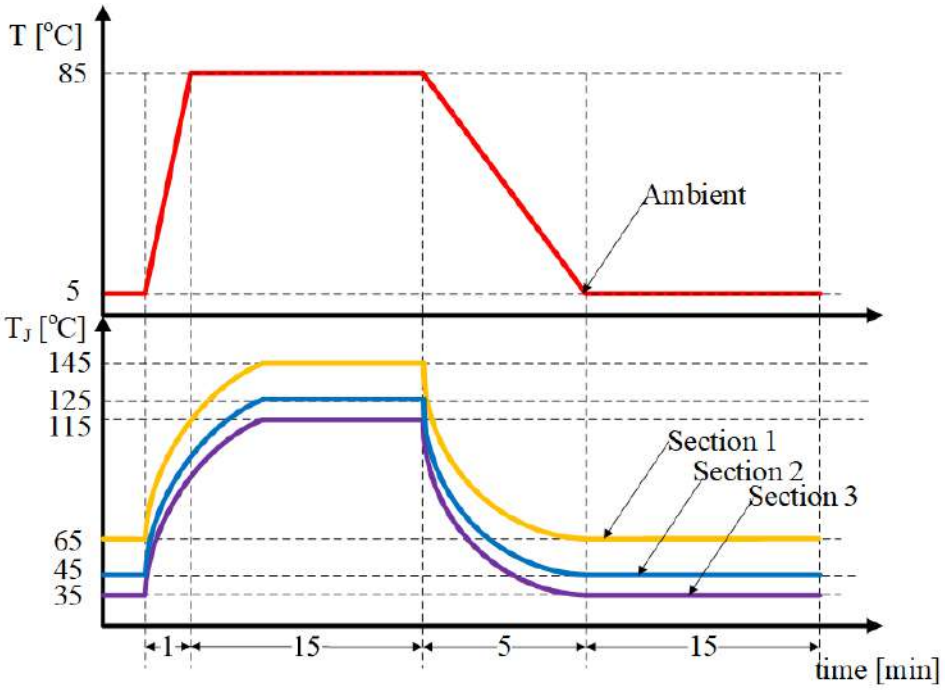

Figure 55. Temperature profile chosen for simplified ALT of driver circuits [199].

The Reliability-Oriented Comparative Test (ROCT) is a simplified version of ALT, which also has to be optimized for the particular failure or degradation mechanism. However, the ROCT does not provide any information about absolute MTBF or UL of tested component. Instead, it allows to distinguish which device - among samples subjected to ROCT - is the most durable for particular failure or degradation mechanism. In presented example [199], power MOSFET driver circuits in $SOIC-8$ housing were subjected to the Temperature and Power Cycling (TPC) test, based on the JESD22-A104E and JESD22-A100D [200, 201] standards. The TPC was found as the most similar to the

real-life operating conditions of the HPPS. The ambient temperature swing was set to $80°C$ (from $5°C$ to $85°C$), and three set of loads were prepared to introduce high power losses inside DUTs. The test profile is depicted in Fig. 55, while simplified schematic of the laboratory setup is presented in Fig. 56

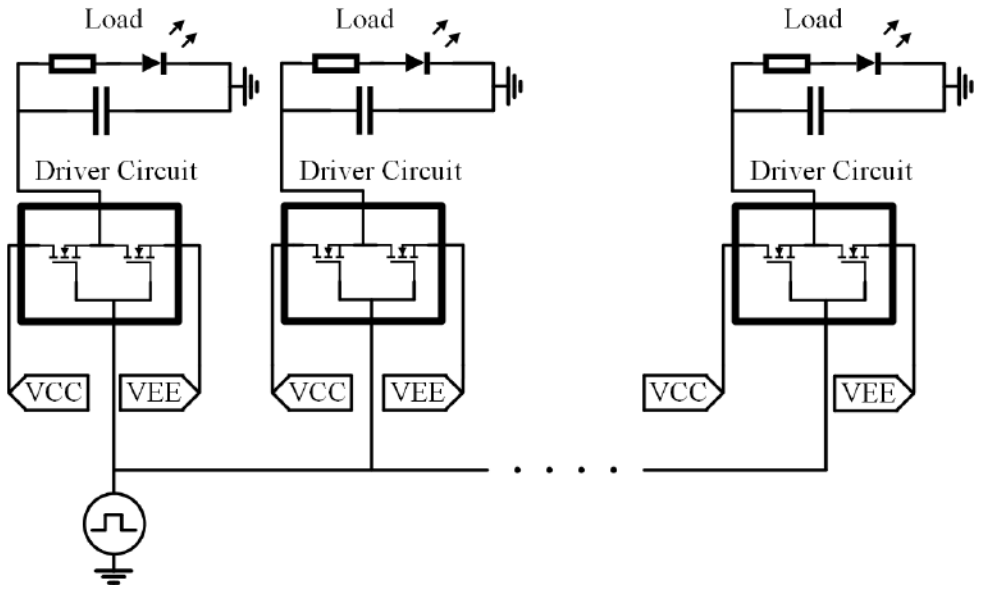

Figure 56. Simplified electrical diagram of the test bench designed for the Reliability-Oriented Comparative Test (ROCT) [199].

The test setup consisted of 108 driver circuits grouped into 6 sets, as it is presented in Tab. 14. All DUTs were operating with high switching frequency (100 kHz) and were connected to the capacitive-resistive load. Sections 1, 2 and 3 were connected to the 30 nF, 20 nF and 10 nF capacitive load accordingly. To simplify the maintenance procedure, a light emitting diode was connected in parallel to each load - the failure was indicated by the Light-Emitting Diode (LED) turn off. The EoL criteria for tested driver circuits were defined as follows:

- fatal failure,
- constant on-state,
- constant off-state,
- improper shape of output signal,
- increase of voltage drop across DUT by 20%.

Table 14. Load and stress conditions defined for tested samplesets [199].

Vendor	Lot Size	Load	$T_{C_{MAX}}$
$[-]$	$[-]$	$[nF]$	$[°C]$
A	18	10	55
B	18	10	55
A	18	20	65
B	18	20	65
A	18	30	85
B	18	30	85

Table 15. Test results - number of failures recorded during test per sampleset [199].

Section	Vendor	Lot	T_C Swing	Faults
$[-]$	$[-]$	$[-]$	$[°C]$	$[-]$
$1A$	A	18	$65-145$	0
$1B$	B	18	$65-145$	0
$2A$	A	18	$35-115$	0
$2B$	B	18	$35-115$	3
$3A$	A	18	$45-125$	0
$3B$	B	18	$45-125$	0

After 1500 thermal cycles, the test was finished and each DUT was subjected to careful laboratory analysis to verify if any of tested samples have met EoL criteria. During the discussed examination, 3 failed samples from vendor B were found. All failed samples were working with the 20 nF capacitive load. Laboratory analysis allowed to distinguish following failure modes:

- internal short circuit between VCC and VEE pin, which led to burnout of the $SOIC-8$ package,
- failure of single switch in the push-pull driver's circuit output, which led to improper shape of the output signal - only the negative voltage was supplied to the load.

Correct and incorrect shape of driver circuit output signal are presented in Figs. 57a) and 57b) respectively. In the case of the faulty driver, positive half-period of driver's output signal was heavily distorted - decreased to $\sim 1\ V$ instead of $12\ V$. However,

negative half-period was not distorted, which suggests that failure was related to burnout of the low-side switch in the driver circuit. Such failure, although did not resulted in the burnout, would cause an improper operation of the power semiconductor device - it would not turn on. Thus, this failure mode would end up in malfunction of HPPS.

Summarizing, 3 out of 54 samples from old supplier were damaged, while none of 54 new counterparts from the new vendor have failed (see Tab. 15). The discussed test proved that the new type of power MOSFET driver circuit is more durable, for the TPC, than the previously used component. This suggests that the replacement of driver circuits B with the driver circuits A should not negatively affect reliability of the HPPS.

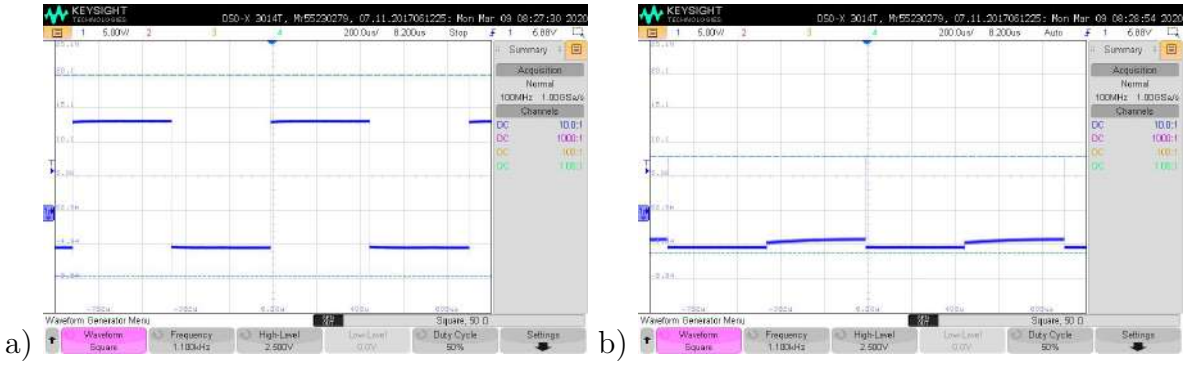

Figure 57. Correct a) and incorrect b) shape of driver output signal [199]. Result indicates failure (short circuit) of a low-side MOSFET in driver circuit.

4.3 Conclusions

In this chapter, a case study analysis for a modified DfR procedure is given. Discussion over design of Power Electronic Building Block (PEBB) module for PEBB-based power converters allows to analyse purpose and scope of:

1. boundary condition definition,
2. simulation stage,
3. design stage and initial reliability evaluation,
4. Proof of Concept (PoC) laboratory testing.

Moreover, presented evaluation shows that DfR favors modular or PEBB-based designs, as they allow to greatly reduce effort required for reliability assessment. This assumption was proven with, calculations of Useful Lifetime (UL) and Failure Rate (FR) for PEBB-based Buck converter.

In this section, concept of the *reliability maintenance* is also discussed. Discussion stresses out the necessity of thorough testing and qualification procedures for each component, as even the simplest element may easily lower reliability of any complex system - like High Performance Power Supply (HPPS) for plasma processing. To address the issue of industry-friendly, cost-efficient qualification process for electronic components, a concept of a Reliability-Oriented Comparative Test (ROCT) was introduced. Presented test results proves that proposed counterpart of driver circuit has higher reliability, than the previously used one. Thus, usage of tested counterpart will not deteriorate overall reliability of HPPS.

Chapter 5

Summary

5.1 Goals and outcome

To prove this thesis following goals were defined:

1. Analysis of operating conditions of HPPSs for plasma processing systems and power converter topologies used for such applications.
2. Proposal of the DfR procedure, suitable for the development of new HPPSs.
3. Design and start-up of the ALT of SiC MOSFET in $SOT-227B$ housing.
4. Identification of reliability model, based on the ALT results.

Goals defined in 1 were found fulfilled. A detailed analysis of plasma processing techniques and types of plasma systems, given in 1.1, indicates a significant demand for increasing the reliability of High Performance Power Supplies (HPPSs) for plasma processing. The presented analysis covers not only chemical- or physical- aspects of plasma, but also the technical challenges related to the manufacturing processes of semiconductor devices, Flat Panel Displays (FPDs), and Low-E glass. This discussion allows to distinguish two types of plasma systems: batch and in-line, and unique requirements for HPPSs for plasma processing (ability to withstand and suppress arc, supporting a very high du/dt at output voltage, ability to withstand high VSWR). Moreover, typical operating conditions of batch systems cause Power Cycling (PC) of HPPSs in this system. Thus, power semiconductor devices in those HPPSs are subjected

to a heavy thermomechanical load, which may shorten their Useful Lifetime (UL). At last, a taxonomy of HPPSs for plasma processing and evaluation of power converter topologies for such applications is given.

In chapter 2, various strategies or reliability improvement of HPPSs are cross-compared. Presented analysis shows that the Design for Reliability (DfR) concept is most suitable for modern HPPSs. This conclusion was given, as the fault-tolerant design requires module- or component- level redundancy, which increases the size and price of HPPS. Unfortunately, it opposes market demands on price and size reduction of HPPSs for plasma processing. Moreover, fault-handling itself would disrupt the plasma process, which could deteriorate the quality of the processed layer. The Remaining Useful Lifetime (RUL) estimation was challenging in practical realization, due to the variety and number of critical components in modern HPPSs. Moreover, off-line State of Health (SoH) estimation methods brings up concerns about cyber-security and the safety of recorded data. Thus, off-line SoH estimation methods might not be accepted by end-users of HPPSs for plasma processing. At last, reliability modelling was found as part of the DfR concept.

Discussion given in 2 shows that classical DfR is not a valid approach for HPPSs for plasma processing. Thus, a modified DfR procedure, optimized for short lifespan or Time To Market (TTM) projects, was proposed. The presented modification allows to shorten the time required to prepare the Proof of Concept (PoC) of new HPPS, and shifts the pressure from the simulation study to the extensive laboratory testing. Moreover, the modified DfR procedure introduces a concept of *reliability maintenance*, which was not previously addressed.

Presented analysis allows distinguishing the main challenges related to the successful implementation of the modified DfR procedure to the engineering workflow. To address those challenges a set of tasks and workpackages was defined. Next, based on the field reliability data, power semiconductor devices were found as the dominant root-cause of failures in HPPSs for plasma processing. This led to the conclusion that further research shall be focused on power semiconductor devices.

In chapter 3 the whole procedure of identification of SiC power MOSFET reliability model is given. Analysis covers not only cross-comparison of different strategies for Accelerated Lifetime Test (ALT) of SiC power MOSFETs, but also a technical challenges related to the preparation of ALT. To make ALT more industry-friendly, concept of *fatigue-like* failure mode was introduced, which allows to group similar failure modes (bond wire lift-off, bond wire heel cracking, solder joint fatigue, solder delamination) and treat them as one. This approach is much more suitable for some industrial customers of power electronics, as it allows to decrease number of ALTs required to develop a reliability model. According to Eq. 27, Number of Required Tests (N_{TEST}) to identify reliability model is a product of Number of Failure Modes (N_{FM}) and Number of Stressors (N_{STR}). Proposed approach allows to reduce N_{FM} to 1.

$$N_T = N_{FM} \cdot N_S \tag{27}$$

The last goal, which was *„Identification of reliability model, based on the ALT results"* was also fulfilled. Presented analysis proves that Weibull distribution is suitable for reliability modelling of *fatigue-like* failure modes. Moreover, proposed approach of combining a Weibull distribution with a CIPS2008 model, allows to obtain the PDF for various operating conditions. Good fitness of the proposed reliability model to the ALT results, indicates that it might be used for purposes of DfR procedure.

In chapter 4, a case study analysis for a modified DfR procedure is given. For this purpose, a Power Electronic Building Block (PEBB) and PEBB-based power converter were designed. Presented case study shows in practice chosen aspects of modified DfR procedure:

1. boundary condition definition,
2. simulation stage,
3. design stage and initial reliability evaluation,
4. Proof of Concept (PoC) laboratory testing.

In presented case study, Useful Lifetime (UL) of SiC power MOSFETs in $TO-247$ housing used in the PEBB module, was estimated based on the given reliability model. Moreover, the Failure Rate (FR) of power semiconductor devices and foil capacitors was also calculated. Next, case study analysis on the *reliability maintenance* was given. Presented test results show the importance of conducting the Reliability-Oriented Comparative Test (ROCT), as even the slightest change in the design of HPPS may deteriorate its reliability.

Based on the presented results, thesis given in chapter 1 was found correct. Indeed, it is possible to develop a probabilistic model, describing a probability of failure of Silicon Carbide (SiC) power MOSFET, which enables reliability evaluation of newly developed High Performance Power Supply (HPPS) for plasma processing, according to the modified DfR procedure. Moreover, following outcomes are considered as own achievements:

1. Methodology of ALT and Power Cycling (PC) for SiC power MOSFETs in $SOT-227B$ housing.
2. Large scale test bench for PC of SiC power MOSFETs.
3. The gate voltage controller circuit for SiC power MOSFETs subjected to PC test.
4. Method for failure detection of SiC power MOSFETs, suitable for usage in the ALT.
5. Methodology of ROCT for electronic circuits (MOSFET drivers).
6. A multiparameter reliability model for SiC power MOSFET in $SOT-227B$ housing.
7. Modified DfR procedure, optimized for projects with a short lifespan or TTM.
8. Concept of the *reliability maintenance*, as a key aspect of DfR methodology and procedure.
9. Reliability-Oriented Control (ROC) algorithm and the design of a electronic circuit supporting proposed ROC algorithm.

5.2 Areas for further research

Reliability engineering is a broad, multi-disciplinary branch of technical sciences, which will face its renaissance in the field of power electronics. Moreover, based on the presented research and state-of-the-art analysis, it is expected that future trend in this matter will focus on:

- Identification of still unrevealed degradation mechanisms in new generations of power semiconductor and optoelectronic devices. One of the limiting factors is duration of ALTs, which significantly slows the research over new failure modes.
- Standardization of ALT procedures, based on novel reliability models and detailed understanding of degradation mechanisms of power semiconductor devices. This tendency is meant to increase accuracy and reproducibility of ALTs, as well as to shorten they duration.
- The Power Electronic Building Block (PEBB) concept. Modular design is highly favorable choice, from the point of view of the reliability assessment. Thus, increasing awareness about reliability amoung users of HPPSs, and more demanding formal requirements about power electronics reliability, might cause a shift towards PEBB-based designs.

Thus, to ensure that future work will fit to above-mentioned directions, it will be focused on:

- Reliability modelling of power semiconductor devices subjected to the low ΔT_J (below $40°C$).
- Reliability modelling of power semiconductor devices subjected to the PC with different t_{ON} and t_{OFF} ratios.
- PC of power semiconductor devices, where DUTs are subjected to the switching losses instead of conduction losses.
- Highly reliable and robust Power Electronic Building Blocks (PEBBs) for new generations of modular HPPSs.

5.3 Future work related to the modified Design for Reliability (DfR) procedure

Beside research described in previous subsection, much effort will be put on further development of proposed modified DfR procedure. Based on the work packages given in subsection 2.4, following tasks can be determined:

- Development of reliability models for critical components used in the next generations of HPPSs, as well development of industry-friendly ALT methodologies for them. Critical components which requires such effort are e.g.:
  - capacitors,
  - new generations of switching diodes,
  - new generations of junction and field-effect components,
  - $GaN\ HEMT$ devices.
- Development of dedicated tools and measurement procedures, to ensure that during laboratory testing of HPPS, key stressors are estimated with sufficient accuracy, repeatability and reproducibility for each critical component. This addresses the:
  - a ripple current measurement in the bundles of capacitors,
  - a peak and root-mean-square current measurement in the multichip modules or discrete components in complex, packed designs,
  - a junction temperature measurement in the multichip modules or discrete components in complex, packed designs,
  - electrical measurements of power semiconductor devices operating with very high switching frequency (e.g. 4 MHz, 13.56 MHz, 60 MHz), or with very high du/dt.
- Development of Reliability-Oriented Comparative Test (ROCT) procedures for other critical components of modern HPPSs.

Bibliography

[1] Mundotia, R. *et al.*, „Effect of ion bombardment and micro-blasting on the wear resistance properties of hard tin coatings," *Materials Today: Proceedings*, 2020, ISSN: 2214-7853. DOI: https://doi.org/10.1016/j.matpr.2019.12.171. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S2214785319341823.

[2] Cotrut, C., Balaceanu, M., Titorencu, I., Braic, V., and Braic, M., „Zrnbcn thin films as protective layers in biomedical applications," *Surface and Coatings Technology*, vol. 211, pp. 57–61, 2012, Proceedings of Symposium K on Protective Coatings and Thin Films, E-MRS 2011 Conference, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2011.08.016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897211008164.

[3] Abundiz-Cisneros, N., Sanginés, R., Rodríguez-López, R., Peralta-Arriola, M., Cruz, J., and Machorro, R., „Novel low-e filter for architectural glass pane," *Energy and Buildings*, vol. 206, p. 109 558, 2020, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2019.109558. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0378778819300568.

[4] Nagasawa, H., Xu, J., Kanezashi, M., and Tsuru, T., „Atmospheric-pressure plasma-enhanced chemical vapor deposition of uv-shielding tio2 coatings on transparent plastics," *Materials Letters*, vol. 228, pp. 479–481, 2018, ISSN: 0167-577X. DOI: https://doi.org/10.1016/j.matlet.2018.06.053. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167577X18309583.

[5] Durocher-Jean, A., Durán, I. R., Asadollahi, S., Laroche, G., and Stafford, L., „Deposition of anti-fog coatings on glass substrates using the jet of an open-to-air microwave argon plasma at atmospheric pressure," *Plasma Processes and Polymers*, vol. n/a, no. n/a, e1900229, 2020. DOI: 10.1002/ppap.201900229. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/ppap.201900229. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/ppap.201900229.

[6] Gledhill, S., Steyer, K., Weiss, C., and Hildebrandt, C., „Hipims and dc magnetron sputter-coated silver films for high-temperature durable reflectrors," *Coatings*, 2019.

[7] Gupta, P. *et al.*, „Decorative black coatings on titanium surfaces based on hard bi-layered carbon coatings synthesized by carbon implantation," *Surface and Coatings Technology*, vol. 358, pp. 386–393, 2019, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2018.11.060. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897218312702.

[8] Silva Oliveira, C. da *et al.*, „Zr-o-n coatings for decorative purposes: Study of the system stability by exploration of the deposition parameter space," *Surface and Coatings Technology*, vol. 343, pp. 30–37, 2018, Selected papers of the "E-MRS 2017 – Symposium Q", ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2017.11.056. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897217312033.

[9] Chen, L. *et al.*, „Metal-dielectric pure red to gold special effect coatings for security and decorative applications," *Surface and Coatings Technology*, vol. 363, pp. 18–24, 2019, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2019.01.098. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S025789721930115X.

[10] Kogelschatz, U., Eliasson, B., and Egli, W., „From ozone generators to flat television screens: History and future potential of dielectric-barrier discharges," *Pure and Applied Chemistry*, vol. 71, no. 10, pp. 1819–1828, 1999.

[11] Zhang, L., Wang, H., and Luo, H., „Uncovering the inactivation kinetics of escherichia coli in saline by atmospheric dbd plasma using atr ft-ir," *Plasma Processes and Polymers*, vol. n/a, no. n/a, e1900197, 2020. DOI: 10.1002/ppap.201900197. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/ppap.201900197. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/ppap.201900197.

[12] Brandenburg, R., „Dielectric barrier discharges: Progress on plasma sources and on the understanding of regimes and single filaments," *Plasma Sources Science and Technology*, vol. 26, no. 5, p. 053 001, Mar. 2017. DOI: 10.1088/1361-6595/aa6426.

[13] Kim, K. N., Lee, S. M., Mishra, A., and Yeom, G. Y., „Atmospheric pressure plasmas for surface modification of flexible and printed electronic devices: A review," *Thin Solid Films*, vol. 598, pp. 315–334, 2016, ISSN: 0040-6090. DOI: https://doi.org/10.1016/j.tsf.2015.05.035. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0040609015005696.

[14] Talalaev, R., „22 - transport phenomena in vapor phase epitaxy reactors," in *Handbook of Crystal Growth (Second Edition)*, Second Edition, ser. Handbook of Crystal Growth. Boston: North-Holland, 2015, pp. 909–942, ISBN: 978-0-444-63304-0. DOI: https://doi.org/10.1016/B978-0-444-63304-0.00022-6. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780444633040000226.

[15] Svavil'nyi, M., Panarin, V., Shkola, A., Nikolenko, A., and Strelchuk, V., „Plasma enhanced chemical vapor deposition synthesis of graphene-like structures from plasma state of co2 gas," *Carbon*, 2020, ISSN: 0008-6223. DOI: https://doi.org/10.1016/j.carbon.2020.05.057. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S000862232030498X.

[16] Shi, Y., Wang, Y., Ren, Y., and Sang, Z., „Effects of the oxide layer with different thicknesses on copper substrate on depressing graphene nucleation by low pressure chemical vapor deposition," *Journal of Crystal Growth*, vol. 541, p. 125 682, 2020, ISSN: 0022-0248. DOI: https://doi.org/10.1016/j.jcrysgro.2020.125682. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0022024820302050.

[17] Zilko, J. L., „4 - metal organic chemical vapor deposition: Technology and equipment," in *Handbook of Thin Film Deposition Processes and Techniques (Second Edition)*, Seshan, K., Ed., Second Edition, Norwich, NY: William Andrew Publishing, 2001, pp. 151–203, ISBN: 978-0-8155-1442-8. DOI: https://doi.org/10.1016/B978-081551442-8.50009-2. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780815514428500092.

[18] Toral, T. R. and Krausse, D., „High power dual frequency systems for next generation display applications - advantages, opportunities and challenges," in *10th International Conference on Power Electronics for Plasma Engineering*, 2019, pp. 77–80.

[19] Chen, S.-H., Živný, O., Mašláni, A., and Chau, S.-W., „Abatement of fluorinated compounds in thermal plasma flow," *Journal of Fluorine Chemistry*, vol. 217, pp. 41–49, 2019, ISSN: 0022-1139. DOI: https://doi.org/10.1016/j.jfluchem.2018.10.004. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0022113918301908.

[20] **Baba, S.**, Gajewski, W., Jasinski, M., Zelechowski, M., and Kazmierkowski, M. P., „High performance power supplies for plasma materials processing," *IEEE Access*, pp. 1–1, 2021. DOI: 10.1109/ACCESS.2021.3054051.

[21] Laermer, F., Franssila, S., Sainiemi, L., and Kolari, K., „Chapter 16 - deep reactive ion etching," in *Handbook of Silicon Based MEMS Materials and Technologies (Third Edition)*, ser. Micro and Nano Technologies, Tilli, M., Paulasto-Krockel, M., Petzold, M., Theuss, H., Motooka, T., and Lindroos, V., Eds., Third Edition, Elsevier, 2020, pp. 417–446, ISBN: 978-0-12-817786-0. DOI: https://doi.org/10.1016/B978-0-12-817786-0.00016-5. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780128177860000165.

[22] Ren, Z. and McNie, M. E., „Inductively coupled plasma etching of tapered via in silicon for mems integration," *Microelectronic Engineering*, vol. 141, pp. 261–266, 2015, Micro/Nano Fabrication 2014, ISSN: 0167-9317. DOI: https://doi.org/10.1016/j.mee.2015.03.071. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931715002506.

[23] Heikkinen, J. J. *et al.*, „Plasma etched carbon microelectrode arrays for bioelectrical measurements," *Diamond and Related Materials*, vol. 90, pp. 126–134, 2018, ISSN: 0925-9635. DOI: https://doi.org/10.1016/j.diamond.2018.09.024. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0925963518303984.

[24] Wośko, M. *et al.*, „Metalorganic vapour-phase epitaxy of algan/gan heterostructures on chlorine plasma etched gan templates without buried conductive layer," *Materials Science in Semiconductor Processing*, vol. 107, p. 104 816, 2020, ISSN: 1369-8001. DOI: https://doi.org/10.1016/j.mssp.2019.104816. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369800119314246.

[25] Addonizio, M., Antonaia, A., and Fusco, L., „Plasma etched c-si wafer with proper pyramid-like nanostructures for photovoltaic applications," *Applied Surface Science*, vol. 467-468, pp. 143–150, 2019, ISSN: 0169-4332. DOI: https://doi.org/10.1016/j.apsusc.2018.10.078. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0169433218327764.

[26] Mattox, D. M., „5 - vacuum evaporation and vacuum deposition," in *Handbook of Physical Vapor Deposition (PVD) Processing*, Mattox, D. M., Ed., Westwood, NJ: William Andrew Publishing, 1998, pp. 288–342, ISBN: 978-0-8155-1422-0. DOI: https://doi.org/10.1016/B978-081551422-0.50006-1. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780815514220500061.

[27] Saager, S., Scheffel, B., and Heinß, J.-P., „High-rate deposition of high-pure silicon thin films for pv-absorber layers by crucible-free electron beam physical vapor deposition," *Surface and Coatings Technology*, vol. 378, p. 125 019, 2019, ISSN:

0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2019.125019. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897219310102.

[28] Mattox, D. M., „Handbook of physical vapor deposition (pvd) processing (second edition),” in Mattox, D. M., Ed., Second Edition, Boston: William Andrew Publishing, 2010, pp. 237–286, ISBN: 978-0-8155-2037-5. DOI: https://doi.org/10.1016/B978-0-8155-2037-5.00007-1. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780815520375000071.

[29] Lofaj, F., Kabátová, M., Dobrovodský, J., and Cempura, G., „Hydrogenation and hybridization in hard w-c:h coatings prepared by hybrid pvd-pecvd method with methane and acetylene,” *International Journal of Refractory Metals and Hard Materials*, vol. 88, p. 105 211, 2020, ISSN: 0263-4368. DOI: https://doi.org/10.1016/j.ijrmhm.2020.105211. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0263436819304652.

[30] Tiron, V. *et al.*, „Overcoming the insulating materials limitation in hipims: Ion-assisted deposition of dlc coatings using bipolar hipims,” *Applied Surface Science*, vol. 494, pp. 871–879, 2019, ISSN: 0169-4332. DOI: https://doi.org/10.1016/j.apsusc.2019.07.239. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0169433219322755.

[31] Bellido-Gonzalez, V. *et al.*, „Hipims in full face erosion circular cathode for semiconductor applications,” in *2015 IEEE 17th Electronics Packaging and Technology Conference (EPTC)*, Dec. 2015, pp. 1–5. DOI: 10.1109/EPTC.2015.7412263.

[32] Bárdos, L. and Baránková, H., „Cold atmospheric plasma: Sources, processes, and applications,” *Thin Solid Films*, vol. 518, no. 23, pp. 6705–6713, 2010, ISSN: 0040-6090. DOI: https://doi.org/10.1016/j.tsf.2010.07.044. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0040609010009946.

[33] Tendero, C., Tixier, C., Tristant, P., Desmaison, J., and Leprince, P., „Atmospheric pressure plasmas: A review,” *Spectrochimica Acta Part B: Atomic Spectroscopy*, vol. 61, no. 1, pp. 2–30, 2006, ISSN: 0584-8547. DOI: https://doi.org/10.1016/j.sab.2005.10.003. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0584854705002843.

[34] Jaworek, A., Marchewicz, A., Sobczyk, A., Krupa, A., and Czech, T., „Two-stage electrostatic precipitators for the reduction of pm2.5 particle emission,” *Progress in Energy and Combustion Science*, vol. 67, pp. 206–233, 2018, ISSN: 0360-1285. DOI: https://doi.org/10.1016/j.pecs.2018.03.003. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0360128517301703.

[35] Suslov, N., „Plasma-generating device, plasma surgical device and use of plasma surgical device," US8109928B2, Feb. 2012.

[36] Fanelli, F. and Fracassi, F., „Atmospheric pressure non-equilibrium plasma jet technology: General features, specificities and applications in surface processing of materials," *Surface and Coatings Technology*, vol. 322, pp. 174–201, 2017, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2017.05.027. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897217304954.

[37] Wurm, S., „Sematech pushes extreme uv lithography forward," Jan. 2006. DOI: 10.1117/2.1200602.0079.

[38] Perlitz, S. *et al.*, „Actinic review of euv masks: Status and recent results of the aims euv system," vol. 9422, Mar. 2015. DOI: 10.1117/12.2086265.

[39] Agarwal, A. *et al.*, „Effect of simultaneous source and bias pulsing in inductively coupled plasma etching," *Journal of Applied Physics*, vol. 106, no. 10, p. 103 305, 2009. DOI: 10.1063/1.3262616.

[40] Hovsepian, P., Reinhard, C., and Ehiasarian, A., „Cralyn/crn superlattice coatings deposited by the combined high power impulse magnetron sputtering/unbalanced magnetron sputtering technique," *Surface and Coatings Technology*, vol. 201, no. 7, pp. 4105–4110, 2006, Proceedings of the 33rd International Conference on Metallurgical Coatings and Thin Films, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2006.08.027. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897206008371.

[41] Ehiasarian, A. P., Wen, J. G., and Petrov, I., „Interface microstructure engineering by high power impulse magnetron sputtering for the enhancement of adhesion," *Journal of Applied Physics*, vol. 101, no. 5, p. 054 301, 2007. DOI: 10.1063/1.2697052.

[42] Gajewski, W., Ruda, K., Rozanski, P., and Ozimek, P., „Newest achievements with bipolar power supplies in dual magnetron processes," in *2015 Technical Conference Proceedings on Large Area Coating*, 2015.

[43] Richter, F. *et al.*, „Ion energy distributions in azo magnetron sputtering from planar and rotatable magnetrons," *Surface and Coatings Technology*, vol. 204, no. 6, pp. 845–849, 2009, ICMCTF 2009, ISSN: 0257-8972. DOI: https://doi.org/10.1016/j.surfcoat.2009.09.034. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0257897209007336.

[44] Banna, S. *et al.*, „Inductively coupled pulsed plasmas in the presence of synchronous pulsed substrate bias for robust, reliable, and fine conductor etching," *IEEE Transactions on Plasma Science*, vol. 37, no. 9, pp. 1730–1746, 2009.

[45] Baek, J., Kim, J., Lee, J., Park, M., and Moon, G., „A new standby structure integrated with boost pfc converter for server power supply," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5283–5293, 2019. DOI: 10.1109/TPEL.2018.2871138.

[46] Bellec, Q., Le Claire, J., Benkhoris, M. F., and Coulibaly, P., „Power factor correction and dc voltage control limits for arc welding application using pulsed current," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 1406–1411.

[47] Xu, H., Chen, D., Xue, F., and Li, X., „Optimal design method of interleaved boost pfc for improving efficiency from switching frequency, boost inductor, and output voltage," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6088–6107, 2019. DOI: 10.1109/TPEL.2018.2872427.

[48] Zeng, H. and Zhang, J., „An improved control scheme for buck pfc converter for high efficiency adapter application," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4569–4576. DOI: 10.1109/ECCE.2012.6342199.

[49] Alaql, F. and Batarseh, I., „Review and comparison of resonant dc-dc converters for wide-input voltage range applications," in *2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE)*, 2019, pp. 453–458.

[50] Kushwaha, R. and Singh, B., „An improved sepic pfc converter for electric vehicle battery charger," in *2019 IEEE Industry Applications Society Annual Meeting*, 2019, pp. 1–8. DOI: 10.1109/IAS.2019.8912344.

[51] Zhao, B., Abramovitz, A., and Smedley, K., „Family of bridgeless buck-boost pfc rectifiers," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6524–6527, 2015. DOI: 10.1109/TPEL.2015.2445779.

[52] Kolar, J. W. and Friedli, T., „The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013. DOI: 10.1109/TPEL.2012.2197867.

[53] Gong, X., Wang, G., and Bhardwaj, M., „6.6kw three-phase interleaved totem pole pfc design with 98.9% peak efficiency for hev/ev onboard charger," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2029–2034. DOI: 10.1109/APEC.2019.8722110.

[54] Jiang, S., Liu, G., Wang, W., and Xu, D., „Research on bridgeless boost pfc with soft-switching," in *2009 IEEE Vehicle Power and Propulsion Conference*, 2009, pp. 1461–1464. DOI: 10.1109/VPPC.2009.5289522.

[55] Friedli, T., Hartmann, M., and Kolar, J. W., „The essence of three-phase pfc rectifier systems—part ii," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 543–560, 2014. DOI: 10.1109/TPEL.2013.2258472.

[56] Huang, Q. and Huang, A. Q., „Review of gan totem-pole bridgeless pfc," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 187–196, 2017. DOI: 10.24295/CPSSTPEA.2017.00018.

[57] Kumar, A. and Chatterjee, D., „A survey on space vector pulse width modulation technique for a two-level inverter," in *2017 National Power Electronics Conference (NPEC)*, 2017, pp. 78–83. DOI: 10.1109/NPEC.2017.8310438.

[58] Kwon, M. and Lee, W., „A study on the analysis and control of no-load characteristics of llc resonant converter for plasma process," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, May 2018, pp. 114–117. DOI: 10.23919/IPEC.2018.8507871.

[59] Eom, T.-H., Shin, M.-H., Park, Y.-H., Kim, D.-S., Kim, Y.-R., and Won, C.-Y., „Design of bipolar pulse power supply based on llc resonant converter for reactive sputtering process," in *2016 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, Jun. 2016, pp. 391–396. DOI: 10.1109/ITEC-AP.2016.7512984.

[60] Villegas, P. J., Martín-Ramos, J. A., Pernía, A. M., Prieto, M. J., Fernández, D. B., and Marcos-Robredo, G., „High voltage resonant converter to generate plasma in open air," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, P.1–P.7. DOI: 10.23919/EPE.2019.8915423.

[61] Jafari, H. and Habibi, M., „High-voltage charging power supply based on a lcc-type resonant converter operating at continuous conduction mode," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019, ISSN: 1941-0107. DOI: 10.1109/TPEL.2019.2946876.

[62] Mishima, T., Ooue, Y., Fukumoto, Y., and Nakaoka, M., „A secondary-side phase-shifting zvs-pwm dual full bridge dc-dc front-end converter for plasma rf power generator," in *2009 International Conference on Electrical Machines and Systems*, Nov. 2009, pp. 1–6. DOI: 10.1109/ICEMS.2009.5382822.

[63] Li, C. and Xu, D., „Family of enhanced zcs single-stage single-phase isolated ac–dc converter for high-power high-voltage dc supply," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3629–3639, May 2017, ISSN: 1557-9948. DOI: 10.1109/TIE.2017.2652374.

[64] Mnich, A. W., „Power supply with extended output voltage intended for the electric welding and cutting," in *2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2016, pp. 444–449.

[65] Martín-Ramos, J. A., Pardo-Vaquero, O., Díaz, J., Nuño, F., Villegas, P. J., and Martín-Pernía, A., „Modelling a multilevel lcc resonant ac-dc converter for wide variations in the input and the load," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5217–5228, Jun. 2019, ISSN: 1941-0107. DOI: 10.1109/TPEL.2018.2867287.

[66] Michaels, J. V. and Wood, W. P., *Design to cost*. John Wiley & Sons, 1989, vol. 3.

[67] Edson, B. and Xijin Tian, „A prediction based design-for-reliability tool," in *Annual Symposium Reliability and Maintainability, 2004 - RAMS*, Jan. 2004, pp. 412–417. DOI: 10.1109/RAMS.2004.1285484.

[68] Madarász, R. R., Kelemen, A., and Fekete, A., „Plasma ignition and current control considerations for magnetron sputtering power supplies," in *2018 International IEEE Conference and Workshop in Óbuda on Electrical and Power Engineering (CANDO-EPE)*, Nov. 2018, pp. 27–32. DOI: 10.1109/CANDO-EPE.2018.8601148.

[69] Ram, S. K., Abhishek, A., Pedapati, P. K., Verma, B. K., Dhakar, A. K., and Varma, R., „Development of high voltage pulse power supply for microwave tube applications," in *2017 14th IEEE India Council International Conference (INDICON)*, 2017, pp. 1–5.

[70] Nami, A., Sakamoto, T., Akiyama, H., and Akiyama, M., „A capacitor charging power supply for repetitive pulsed power systems," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–9.

[71] Mamun, M. A. A., Furuta, H., and Hatta, A., „Pulsed dc plasma cvd system for the deposition of dlc films," *Materials Today Communications*, vol. 14, pp. 40–46, 2018, ISSN: 2352-4928. DOI: https://doi.org/10.1016/j.mtcomm.2017.12.008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S2352492817303331.

[72] Sochugov, N. S., Oskirko, V. O., and Spirin, R. E., „A power supply for magnetron sputtering systems," *Instruments and Experimental Techniques*, vol. 56, no. 2, pp. 178–184, 2013.

[73] Ozimek, P., Bugyi, R., Dziuba, R., Klimczak, A., and Zelechowski, M., „Reducing stored electrical energy in a lead inductance," English, US9818579, 2017.

[74] Saleh, S. A., Allen, B., Ozkop, E., and Colpitts, B. G., „Multistage and multilevel power electronic converter-based power supply for plasma dbd devices," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5466–5475, Jul. 2018, ISSN: 1557-9948. DOI: 10.1109/TIE.2017.2777379.

[75] Scholtz, J. S., Fontana, L. C., and Mezaroba, M., „Asymmetric bipolar plasma power supply to increase the secondary electrons emission in capacitive coupling plasmas," *IEEE Transactions on Plasma Science*, vol. 46, no. 8, pp. 2999–3007, Aug. 2018, ISSN: 1939-9375. DOI: 10.1109/TPS.2018.2851071.

[76] Cunbo, J., Chunlei, X., Lihong, C., and Xile, W., „Design of high-isolation dc power supply for the cascaded high voltage pulse power," in *2013 5th International Conference on Intelligent Human-Machine Systems and Cybernetics*, vol. 1, 2013, pp. 580–583.

[77] Yang, Y. and Lee, W., „A dc-pulse power supply designed for plasma applications," in *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Nov. 2009, pp. 1086–1090. DOI: 10.1109/PEDS.2009.5385915.

[78] Drummond, G. N. and Scholl, R. A., „Enhanced reactive dc sputtering system," US6001224A, Dec. 1999.

[79] Drummond, G. and Scholl, R. A., „Periodically clearing thin film plasma processing system," US6521099B1, Feb. 2003.

[80] Zhao, Q., Li, S., Cao, R., Wang, D., and Yuan, J., „Design of pulse power supply for high-power semiconductor laser diode arrays," *IEEE Access*, vol. 7, pp. 92 805–92 812, 2019.

[81] Inventor not filed yet, „Plasma power supply having a protection circuit," EP1272014A1, 2003.

[82] Owen, C. M. and Chawla, Y. K., „Variable class characteristic amplifier," US8344801B2, 2013.

[83] de Vries, I. D., van Nierop, J. H., and Greene, J. R., „Solid state class de rf power source," in *IEEE International Symposium on Industrial Electronics. Proceedings. ISIE'98 (Cat. No.98TH8357)*, vol. 2, 1998, 524–529 vol.2.

[84] Yuzurihara, I., Kikuchi, M., Suenaga, T., and Ishikawa, Y., „Power supply apparatus for generating plasma," US20040032212A1, Feb. 2004.

[85] Kirchmeier, T., „Plasma power supply," WO2010022749A1, Mar. 2010.

[86] **Baba, S.**, Gieraltowski, A., Jasinski, M. T., Blaabjerg, F., Bahman, A. S., and Zelechowski, M., „Active power cycling test bench for sic power mosfets - principles, design and implementation," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.

[87] Glueck, M., Miller, A., and Pivit, E., „Rf power supply," US8154897B2, 2012.

[88] Iwasiewicz, A., *Zarzadzanie Jakoscia: podstawowe problemy i metody*. Wydawnictwo Naukowe PWN, 2005.

[89] Zhang, W., Xu, D., Enjeti, P. N., Li, H., Hawke, J. T., and Krishnamoorthy, H. S., „Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, 2014. DOI: 10.1109/TPEL.2014.2304561.

[90] Zhuang, Y., Liu, F., Zhang, X., Huang, Y., Zha, X., and Liu, Z., „Short-circuit fault-tolerant topology for multiport cascaded dc/dc converter in photovoltaic power generation system," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 549–561, 2021. DOI: 10.1109/TPEL.2020.3004070.

[91] Selvaraj, R., Desingu, K., Chelliah, T. R., Khare, D., and Bharatiraja, C., „Fault tolerant operation of parallel-connected 3l-neutral-point clamped back-to-back converters serving to large hydro-generating units," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5429–5443, 2018. DOI: 10.1109/TIA.2018.2851581.

[92] Selvaraj, G., Sadat, A. R., Krishnamoorthy, H. S., and Rajashekara, K., „An improved fault-tolerant power converter for electric vehicle propulsion," in *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020, pp. 1–5. DOI: 10.1109/PESGRE45664.2020.9070596.

[93] Sang, Z. *et al.*, „Fault tolerant design for cascaded h-bridge multi-level converter based electronic power transformer," in *2018 13th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2018, pp. 2280–2284. DOI: 10.1109/ICIEA.2018.8398090.

[94] van der Broeck, C. H., Polom, T., Lorenz, R. D., and De Doncker, R. W., „Thermal monitoring of power electronic modules using device self-sensing," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4699–4706. DOI: 10.1109/ECCE.2018.8558341.

[95] Soliman, H., Wang, H., and Blaabjerg, F., „A review of the condition monitoring of capacitors in power electronic converters," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4976–4989, 2016. DOI: 10.1109/TIA.2016.2591906.

[96] Jain, P., Poon, J., Singh, J. P., Spanos, C., Sanders, S. R., and Panda, S. K., „A digital twin approach for fault diagnosis in distributed photovoltaic systems," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 940–956, 2020.

[97] Raveendran, V., Andresen, M., Liserre, M., and Buticchi, G., „Lifetime-based power routing of smart transformer with chb and dab converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3523–3529. DOI: 10.1109/APEC.2018.8341612.

[98] Holzke, W., Brunko, A., Groke, H., Kaminski, N., and Orlik, B., „A condition monitoring system for power semiconductors in wind energy plants," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–7.

[99] Raveendran, V., Andresen, M., and Liserre, M., „Improving onboard converter reliability for more electric aircraft with lifetime-based control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5787–5796, Jul. 2019, ISSN: 0278-0046. DOI: 10.1109/TIE.2018.2889626.

[100] Hinz, M., „Condition monitoring system: Approach and application," in *4th Computational Reliability Engineering (CRE) in Product Development and Manufacturing*, 2018.

[101] Hinz, M., Brueggemann, D., and Bracke, S., „Comparison of inductive learning and neural networks in condition monitoring systems of complex machines," Jan. 2019, pp. 1141–1147. DOI: 10.3850/978-981-11-2724-3_0338-cd.

[102] Ugur, E., Xu, C., Yang, F., Pu, S., and Akin, B., „A new complete condition monitoring method for sic power mosfets," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 2, pp. 1654–1664, 2021. DOI: 10.1109/TIE.2020.2970668.

[103] Erturk, F., Ugur, E., Olson, J., and Akin, B., „Real-time aging detection of sic mosfets," *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 600–609, Jan. 2019, ISSN: 0093-9994. DOI: 10.1109/TIA.2018.2867820.

[104] Zhao, Z., Davari, P., Lu, W., Wang, H., and Blaabjerg, F., „An overview of condition monitoring techniques for capacitors in dc-link applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3692–3716, 2021. DOI: 10.1109/TPEL.2020.3023469.

[105] Benecke, F., „Digitalization of industrial vacuum coating - automated process control and data analysis," in *10th International Conference on Power Electronics for Plasma Engineering*, 2019, pp. 10–10.

[106] Engelstadter, J. P., Reinke, I., and Schweizer, M., „Iot services - connected benefits for," in *10th International Conference on Power Electronics for Plasma Engineering*, 2019, pp. 10–10.

[107] Peyghami, S., Wang, H., Davari, P., and Blaabjerg, F., „Mission profile based power converter reliability analysis in a dc power electronic based power system," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 4122–4128. DOI: 10.1109/ECCE.2018.8557552.

[108] Shi, X. and Bazzi, A. M., „Solar photovoltaic power electronic systems: Design for reliability approach," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–8. DOI: 10.1109/EPE.2015.7309352.

[109] Kececioglu, D., *Reliability Engineering Handbook*. Englewood Cliffs, New Jersey: Prentice Hall Inc., 1991, vol. 1.

[110] **Baba, S.**, Bachman, S., Jasinski, M., and Zelechowski, M., „Wbg-based pebb module for high reliability power converters," *IEEE Access*, vol. 9, pp. 86 488–86 499, 2021. DOI: 10.1109/ACCESS.2021.3089045.

[111] „Samsung confirms battery faults as cause of note 7 fires," *BBC News*, Jan. 2017. [Online]. Available: https://www.bbc.com/news/business-38714461.

[112] WIMA, „Foil capacitor reliability," in *http://wima.cn/EN/reliability.htm*.

[113] TDK, „Film capacitors - quality," 2018.

[114] Elerath, J. G., „Afr: Problems of definition, calculation and measurement in a commercial environment," in *Annual Reliability and Maintainability Symposium. 2000 Proceedings. International Symposium on Product Quality and Integrity (Cat. No.00CH37055)*, 2000, pp. 71–76. DOI: 10.1109/RAMS.2000.816286.

[115] „An2019-05 rev. 2.11," Infineon, Tech. Rep., 2019.

[116] Ceccarelli, L., Reigosa, P., Iannuzzo, F., and Blaabjerg, F., „A survey of sic power mosfets short-circuit robustness and failure mode analysis," *Microelectronics Reliability*, vol. 76-77, pp. 272–276, 2017, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2017.06.093. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271417302822.

[117] Wei, J. *et al.*, „Comprehensive analysis of electrical parameters degradations for sic power mosfets under repetitive short-circuit stress," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5440–5447, Dec. 2018, ISSN: 0018-9383. DOI: 10.1109/TED.2018.2873672.

[118] Agarwal, A., Fatima, H., Haney, S., and Ryu, S., „A new degradation mechanism in high-voltage sic power mosfets," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 587–589, 2007. DOI: 10.1109/LED.2007.897861.

[119] Kusumoto, O. *et al.*, „Reliability of diode-integrated sic power mosfet(diomos)," *Microelectronics Reliability*, vol. 58, pp. 158–163, 2016, Reliability Issues in Power Electronics, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2015.11.033. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S002627141530247X.

[120] Fu, H., Wei, J., Liu, S., Wu, W., and Sun, W., „Repetitive-avalanche-induced electrical degradation and optimization for 1.2kv 4h-sic mosfets," in *2019 IEEE 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2019, pp. 1–4. DOI: 10.1109/IPFA47161.2019.8984898.

[121] Yen, C. *et al.*, „Oxide breakdown reliability of sic mosfet," in *2019 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2019, pp. 1–3. DOI: 10.1109/WiPDAAsia.2019.8760324.

[122] Cheung, K. P., „Sic power mosfet gate oxide breakdown reliability — current status," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, 2018, 2B.3-1-2B.3–5.

[123] Khanna, R., Amrhein, A., Stanchina, W., Reed, G., and Mao, Z.-H., „An analytical model for evaluating the influence of device parasitics on cdv/dt induced false turn-on in sic mosfets," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 518–525. DOI: 10.1109/APEC.2013.6520259.

[124] Ryu, S.-H., „Sic power mosfet ruggedness," in *ECPE Workshop: Power Semiconductor Robustness - What Kills Power Devices?*, ECPE, Jan. 2020, pp. 1–1.

[125] Luo, H., Iannuzzo, F., Baker, N., Blaabjerg, F., Li, W., and He, X., „Study of current density influence on bond wire degradation rate in sic mosfet modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1622–1632, 2020. DOI: 10.1109/JESTPE.2019.2920715.

[126] Dugal, F. and Ciappa, M., „Study of thermal cycling and temperature aging on pbsnag die attach solder joints for high power modules," in *2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits*, Jun. 2015, pp. 8–8. DOI: 10.1109/IPFA.2015.7224318.

[127] Ciappa, M., „Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 653–667, Mar. 2002. DOI: 10.1016/S0026-2714(02)00042-2..

[128] Choi, U. and Blaabjerg, F., „Separation of wear-out failure modes of igbt modules in grid-connected inverter systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6217–6223, Jul. 2018, ISSN: 0885-8993. DOI: 10.1109/TPEL.2017.2750328.

[129] Franke, J., Zeng, G., Winkler, T., and Lutz, J., „Power cycling reliability results of gan hemt devices," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 467–470.

[130] Hu, Y., Shi, P., Li, H., and Yang, C., „Health condition assessment of base-plate solder for multi-chip igbt module in wind power converter," *IEEE Access*, vol. 7, pp. 72 134–72 142, 2019, ISSN: 2169-3536. DOI: 10.1109/ACCESS.2019.2918029.

[131] Huang, Y., Luo, Y., Xiao, F., and Liu, B., „Failure mechanism of die-attach solder joints in igbt modules under pulse high-current power cycling," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 99–107, Mar. 2019, ISSN: 2168-6777. DOI: 10.1109/JESTPE.2018.2871474.

[132] Dupont, L., Lefebvre, S., Bouaroudj, M., Khatir, Z., Faugieres, J.-C., and Emorine, F., „Ageing test results of low voltage mosfet modules for electrical vehicles," in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1–10. DOI: 10.1109/EPE.2007.4417433.

[133] Li, X. *et al.*, „Failure mechanism of avalanche condition for 1200-v double trench sic mosfet," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 2147–2154, 2021. DOI: 10.1109/JESTPE.2020.2965002.

[134] Karki, U. and Peng, F. Z., „Effect of gate-oxide degradation on electrical parameters of power mosfets," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 764–10 773, Dec. 2018, ISSN: 0885-8993. DOI: 10.1109/TPEL.2018.2801848.

[135] Song, Q. *et al.*, „4h-sic trench mosfet with l-shaped gate," *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 463–466, 2016. DOI: 10.1109/LED.2016.2533432.

[136] Zorn, C. and Kaminski, N., „Acceleration of temperature humidity bias (thb) testing on igbt modules by high bias levels," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 385–388. DOI: 10.1109/ISPSD.2015.7123470.

[137] Pappis, D. and Zacharias, P., „Failure modes of planar and trench sic mosfets under single and multiple short circuits conditions," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, P.1–P.11.

[138] Liu, J., Zhang, G., Wang, B., Li, W., and Wang, J., „Gate failure physics of sic mosfets under short-circuit stress," *IEEE Electron Device Letters*, vol. 41, no. 1, pp. 103–106, 2020.

[139] Vernica, I., Wang, H., and Blaabjerg, F., „Design for reliability and robustness tool platform for power electronic systems - study case on motor drive applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, pp. 1799–1806. DOI: 10.1109/APEC.2018.8341261.

[140] Shen, Y., Chub, A., Wang, H., Vinnikov, D., Liivik, E., and Blaabjerg, F., „Wear-out failure analysis of an impedance-source pv microinverter based on system-level electrothermal modeling," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3914–3927, May 2019, ISSN: 0278-0046. DOI: 10.1109/TIE.2018.2831643.

[141] Midler, C. and Navarre, C., „Project management in the automotive industry," in Wiley, Nov. 2007, pp. 1368–1388, ISBN: 9780470172391. DOI: 10.1002/9780470172391.ch55.

[142] Qiu, Z., Zhang, J., Ning, P., and Wen, X., „Reliability modeling and analysis of sic mosfet power modules," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2017, pp. 1459–1463. DOI: 10.1109/IECON.2017.8216248.

[143] Liu, X., Wang, Y., Song, C., and Qu, H., „Reliability assessment of micro-grid based on markov model," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Oct. 2016, pp. 2434–2437. DOI: 10.1109/APPEEC.2016.7779922.

[144] Gao, D., Hou, J., Liang, K., and Yang, Q., „Fault diagnosis system for electric vehicle charging devices based on fault tree analysis," in *2018 37th Chinese Control Conference (CCC)*, Jul. 2018, pp. 5055–5059. DOI: 10.23919/ChiCC.2018.8482691.

[145] Wang, H., Ma, K., and Blaabjerg, F., „Design for reliability of power electronic systems," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct. 2012, pp. 33–44. DOI: 10.1109/IECON.2012.6388833.

[146] Scheuermann, U. and Schuler, S., „Power cycling results for different control strategies," *Microelectronics Reliability*, vol. 50, no. 9, pp. 1203–1209, 2010, 21st European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2010.07.135. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410004087.

[147] Ziemann, T., Grossner, U., and Neuenschwander, J., „Power cycling of commercial sic mosfets," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 24–31. DOI: 10.1109/WiPDA.2018.8569138.

[148] Durand, C., Klingler, M., Coutellier, D., and Naceur, H., „Power cycling reliability of power module: A survey," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 1, pp. 80–97, 2016. DOI: 10.1109/TDMR.2016.2516044.

[149] Guo, Z., Sprecher, A. F., and Conrad, H., „Crack initiation and growth during low cycle fatigue of pb-sn solder joints," in *1991 Proceedings 41st Electronic Components Technology Conference*, May 1991, pp. 658–666. DOI: 10.1109/ECTC.1991.163950.

[150] Choi, S., Lee, W., and Lee, K., „Delamination lifetime evaluation of ipm by accelerated power cycle test," in *2014 International Conference on Electronics, Information and Communications (ICEIC)*, Jan. 2014, pp. 1–2. DOI: 10.1109/ELINFOCOM.2014.6914451.

[151] Jiang, M. *et al.*, „Finite element modeling of igbt modules to explore the correlation between electric parameters and damage in bond wires," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019.

[152] Sathik, M., Jet, T. K., Gajanayake, C. J., Simanjorang, R., and Gupta, A. K., „Comparison of power cycling and thermal cycling effects on the thermal impedance degradation in igbt modules," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2015, pp. 001 170–001 175. DOI: 10.1109/IECON.2015.7392258.

[153] Galbiati, E., „Reliability evaluation of solder joints in electronics assemblies," in *2017 21st European Microelectronics and Packaging Conference (EMPC) Exhibition*, Sep. 2017, pp. 1–5. DOI: 10.23919/EMPC.2017.8346843.

[154] Medjahed, H., Vidal, P.-E., and Nogarede, B., „Comparison between electromagnetic and thermal stress induced by direct current flow in igbt bond wires," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1–6.

[155] European Center for Power Electronics, „Qualification of power modules for use in power electronics converter units in motor vehicles," in *ECPE Guideline AQG 324*, 2019.

[156] Thoben, M. and Tuellmann, M., „Lifetime testing i (pc principles)," in *ECPE Tutorial: Testing Automotive Power Modules According to the ECPE Guideline AQG 324*, 2021.

[157] Herrmann, T., Feller, M., Lutz, J., Bayerer, R., and Licht, T., „Power cycling induced failure mechanisms in solder layers," in *2007 European Conference on Power Electronics and Applications*, Sep. 2007, pp. 1–7. DOI: 10.1109/EPE.2007.4417702.

[158] International Electrotechnical Commission, *Iec 60749-34:2010 semiconductor devices - mechanical and climatic test methods - part 34: Power cycling*, International Electrotechnical Commission.

[159] Ugur, E., Yang, F., Pu, S., Zhao, S., and Akin, B., „Degradation assessment and precursor identification for sic mosfets under high temp cycling," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2858–2867, May 2019, ISSN: 0093-9994. DOI: 10.1109/TIA.2019.2891214.

[160] Dbeiss, M. and Avenas, Y., „Power semiconductor ageing test bench dedicated to photovoltaic applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 3003–3010, May 2019, ISSN: 0093-9994. DOI: 10.1109/TIA.2019.2897681.

[161] Zhang, J., Qiu, Z., Zhang, E., and Ning, P., „Comparison and analysis of power cycling and thermal cycling lifetime of igbt module," in *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, Oct. 2018, pp. 876–880. DOI: 10.23919/ICEMS.2018.8549346.

[162] Kozak, J. P., Ngo, K. D. T., DeVoto, D. J., and Major, J. J., „Impact of accelerated stress-tests on sic mosfet precursor parameters," in *2018 Second International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Jun. 2018, pp. 1–5. DOI: 10.1109/3DPEIM.2018.8525234.

[163] Ammous, K. *et al.*, „Error in estimation of power switching losses based on electrical measurements," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 1, Jun. 2000, 286–291 vol.1. DOI: 10.1109/PESC.2000.878859.

[164] Krone, T., Dang Hung, L., Jung, M., and Mertens, A., „On-line semiconductor switching loss measurement system for an advanced condition monitoring concept," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10. DOI: 10.1109/EPE.2016.7695546.

[165] Mulpuri, V. and Choi, S., „Reliability of sic power mosfets under high repetitive pulse current conditions," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 776–782. DOI: 10.1109/APEC.2017.7930783.

[166] Fiel, A. and Wu, T., „Mosfet failure modes in the zero-voltage-switched full-bridge switching mode power supply applications," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, vol. 2, Mar. 2001, 1247–1252 vol.2. DOI: 10.1109/APEC.2001.912525.

[167] Schoisohl, J., *Linear mode operation and safe operating diagram of power-mosfets*, 1.1, Infineon Technologies, 2017.

[168] Raee, H., Rabiei, A., and Thirnger, T., „Analytical prediction of switching losses in mosfets for variable drain-source voltage and current applications," in *2013 IEEE 8th Conference on Industrial Electronics and Applications (ICIEA)*, 2013, pp. 705–709. DOI: 10.1109/ICIEA.2013.6566458.

[169] Herold, C., Franke, J., Bhojani, R., Schleicher, A., and Lutz, J., „Requirements in power cycling for precise lifetime estimation," *Microelectronics Reliability*, vol. 58, pp. 82–89, 2016, Reliability Issues in Power Electronics, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2015.12.035. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271415302821.

[170] Herold, C., Sun, J., Seidel, P., Tinschert, L., and Lutz, J., „Power cycling methods for sic mosfets," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, May 2017, pp. 367–370. DOI: 10.23919/ISPSD.2017.7988994.

[171] Lang, F., Yamaguchi, H., Nakagawa, H., and Sato, H., „Deformation and oxidation of copper metallization on ceramic substrate during thermal cycling from -40c to 250c," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 8, pp. 1069–1074, Aug. 2015, ISSN: 2156-3950. DOI: 10.1109/TCPMT.2015.2423612.

[172] Denria, J., Rajmane, P., and Agonafer, D., „Board level solder joint reliability assessment study of megtron 6 vs fr-4 under power cycling and thermal cycling," in *2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, May 2018, pp. 1289–1295. DOI: 10.1109/ITHERM.2018.8419505.

[173] Hanif, A., Das, S., and Khan, F., „Active power cycling and condition monitoring of igbt power modules using reflectometry," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, pp. 2827–2833. DOI: 10.1109/APEC.2018.8341418.

[174] Liao, L.-L., Liu, C.-K., and Chiang, K.-N., „Power cycling test and failure mode analysis of high-power module," in *2016 International Conference on Electronics Packaging (ICEP)*, Apr. 2016, pp. 372–377. DOI: 10.1109/ICEP.2016.7486850.

[175] Sow, A., Somaya, S., Ousten, Y., Vinassa, J.-M., and Patoureaux, F., „Power mosfet active power cycling for medical system reliability assessment," *Microelectronics Reliability*, vol. 53, no. 9, pp. 1697–1702, 2013, European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2013.07.096. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271413002722.

[176] Choi, U., Blaabjerg, F., and Joergensen, S., „Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, Mar. 2018, ISSN: 0885-8993. DOI: 10.1109/TPEL.2017.2690500.

[177] Brandelero, J., Ewanchuk, J., and Mollov, S., „Online junction temperature measurements for power cycling power modules with high switching frequencies," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 2016, pp. 191–194. DOI: 10.1109/ISPSD.2016.7520810.

[178] Zhang, L., Liu, P., Guo, S., and Huang, A. Q., „Comparative study of temperature sensitive electrical parameters (tsep) of si, sic and gan power devices," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2016, pp. 302–307. DOI: 10.1109/WiPDA.2016.7799957.

[179] Liu, P., Chen, C., Zhang, X., and Huang, S., „Online junction temperature estimation method for sic modules with built-in ntc sensor," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 94–99, 2019.

[180] **Baba, S.**, Zelechowski, M., and Jasinski, M., „Estimation of thermal network models parameters based on particle swarm optimization algorithm," in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2019, pp. 1–6.

[181] Bahman, A. S., Ma, K., and Blaabjerg, F., „A lumped thermal model including thermal coupling and thermal boundary conditions for high-power igbt modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2518–2530, 2018.

[182] **Baba, S.**, Jasinski, M., and Zelechowski, M., „Temperature measurement of rf power amplifier," in *2020 19th International Power Electronics and Motion Control Conference*, 2021, pp. 1–1. DOI: -.

[183] Cemernek, D., Gursch, H., and Kern, R., „Big data as a promoter of industry 4.0: Lessons of the semiconductor industry," in *2017 IEEE 15th International Conference on Industrial Informatics (INDIN)*, 2017, pp. 239–244.

[184] **Baba, S.**, „Multiparameter reliability model for sic power mosfets subjected to repetitive thermomechanical load," *Bulletin of the Polish Academy of Sciences: Technical Sciences*, vol. 69, Mar. 2021. DOI: 10.24425/bpasts.2021.137386.

[185] Ma, L., Bao, S., Lv, D., Du, Z., and Li, S., „Application of c-mode scanning acoustic microscopy in packaging," in *2007 8th International Conference on Electronic Packaging Technology*, 2007, pp. 1–6. DOI: 10.1109/ICEPT.2007.4441498.

[186] Zhou, B., Lu, T., and You, J., „Study on fatigue ductility coefficient and life prediction for mixed solder joints under thermal cycle loads," in *2014 10th International Conference on Reliability, Maintainability and Safety (ICRMS)*, Aug. 2014, pp. 686–690. DOI: 10.1109/ICRMS.2014.7107285.

[187] Okada, K., Kurimoto, K., and Suzuki, M., „Intrinsic mechanism of non-linearity in weibull tddb lifetime and its impact on lifetime prediction," in *2015 IEEE International Reliability Physics Symposium*, Apr. 2015, 2A.4.1–2A.4.5. DOI: 10.1109/IRPS.2015.7112671.

[188] Jamin, L., Tao, X., Raymond, C., Orlando, V., and Christoph, L., „Cu and al-cu composite-material interconnects for power devices," May 2012, pp. 1905–1911, ISBN: 978-1-4673-1966-9. DOI: 10.1109/ECTC.2012.6249098.

[189] Bayerer, R., Herrmann, T., Licht, T., Lutz, J., and Feller, M., „Model for power cycling lifetime of igbt modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, Mar. 2008, pp. 1–6.

[190] Lai, W., Chen, M., Ran, L., Alatise, O., Xu, S., and Mawby, P., „Low dtj stress cycle effect in igbt power module die-attach lifetime modeling," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6575–6585, Sep. 2016, ISSN: 0885-8993. DOI: 10.1109/TPEL.2015.2501540.

[191] Chen, Z., Danilovic, M., Boroyevich, D., and Shen, Z., „Modularized design consideration of a general-purpose, high-speed phase-leg pebb based on sic mosfets," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[192] Bachman, S., **Baba, S.**, and Jasiński, M., „A wide-bandgap based power electronic building block for reliable modular power converter," in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, pp. 46–52. DOI: 10.1109/PEMC48073.2021.9432591.

[193] R., G., „Metallized film capacitor lifetime evaluation and failure mode analysis," in *Proceedings of the CAS-CERN Accelerator School: Power Converters*, 2015.

[194] Department of Defense, *Military Handbook: Reliability Prediction of Electronic Equipment*. 1991.

[195] International Electrotechnical Commission, *Iec 62380:2004 reliability data handbook - universal model for reliability prediction of electronics components, pcbs and equipment*, 1.0, International Electrotechnical Commission, Aug. 2004.

[196] ——, *Iec 61709:2017 electric components - reliability - reference conditions for failure rates and stress models for conversion*, 3.0, International Electrotechnical Commission, Feb. 2017.

[197] FIDES, *Fides reliability methodology for electronic systems*, A, 2009.

[198] ERICSSON, *Sr-332 reliability prediction procedure for electronic equipment*, 4th ed., ERICSSON, Mar. 2016.

[199] Wisniewski, J., **Baba, S.**, and Jasinski, M., „Reliability demonstration of high performance power supply after ic vendor replacement," in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, pp. 363–367. DOI: 10.1109/PEMC48073.2021.9432635.

[200] JEDEC, *Jesd22-a104e - temperature cycling*.

[201] ——, *Jesd22-a100d cycled temperature-humidity-bias life test*.

List of Abbreviations and Symbols

AFR Annual Failure Rate 46, 47, 56

AGB Avalanche Gate Breakdown 50

ALT Accelerated Lifetime Test 9, 12, 47, 50, 55, 56, 59–61, 63–66, 69–73, 75–81, 85, 86, 88, 89, 93, 95, 97, 102, 118, 123, 125–128, 164–167, 169

APP Atmospheric Pressure Plasma 9, 13, 14, 19

BJT Bipolar Junction Transistor 71

CC Current Cycling 61–63, 65, 66, 70

CCP Capacitively Coupled Plasma 27

CD Corona Discharge 19–21, 30, 163

CDF Cumulative Density Function 42, 44, 47, 48, 164

CSAM Confocal Scanning Acoustic Microscopy 86, 88, 90, 91, 102, 166

CVD Chemical Vapor Deposition 9, 11, 14, 31, 163

DAB Dual Active Bridge 105

DBD Dielectric Barrier Discharge 19–21, 30, 163

DC Direct Current 11, 16, 18, 24, 25, 30, 31, 69–71, 163

DfR Design for Reliability 9–12, 30, 40–43, 45, 47, 49, 51–59, 80, 94, 97, 99, 102, 105, 106, 109, 112, 113, 115, 117, 121–126, 128, 164

DtC Design to Cost 30, 66

DUT Device Under Test 60, 61, 63, 64, 66, 69–71, 73, 75–77, 80, 85, 88–92, 102, 119, 120, 127, 166

EoL End of Life 9, 45, 47, 61, 62, 64–66, 103, 119, 120, 169

ESP Electrostatic Precipitator 20

EUV Extreme Ultraviolet 23

FEM Finite Element Modelling 79

FIT Failures In Time 45

FPD Flat Panel Displays 23, 123

FR Failure Rate 43, 58, 112, 122, 126

FTA Fault-Tree Analysis 54, 113

HALT Highly-Accelerated Life Test 55

HAR High Aspect Ratio 16

HAST Highly-Accelerated Stress Test 55

HCI Hot Carrier Injection 50

HiPIMS High Power Impulse Magnetron Sputtering 19, 32

HPPS High Performance Power Supply 11, 21, 27, 28, 35, 37–39, 49, 55–58, 62, 63, 79, 80, 117–119, 121, 122, 124, 126, 128

HPPSs High Performance Power Supplies 9, 11, 12, 22, 24, 26, 34, 35, 37, 38, 40–42, 44, 46, 48, 50, 52, 54, 56–58, 123, 124, 127, 128, 163

ICP Inductively Coupled Plasma 16, 27

IGBT Insulated Gate Bipolar Transistor 39, 47, 71–73, 94, 102, 111, 165

ITR Łukasiewicz Tele- and Radio Research Institute 86

KPI Key Performance Indicators 28, 30, 34

LCD Liquid Crystal Display 14, 21

LD Lifetime Distributions 43, 47, 59

LED Light-Emitting Diode 119

LPCVD Low Pressure Chemical Vapor Deposition 14

MD Markov Diagram 54, 113

MF Medium Frequency 25, 26, 31

MLE Maximum Likehood Estimation 94

MOCVD Metal-Organic Chemical Vapor Deposition 14

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor 9, 11, 12, 49, 50, 58–60, 62–82, 84–86, 88, 90, 92, 94, 96, 98, 100, 102, 104, 111, 123, 125, 126, 164, 165, 167, 169

MST Multi-Stressor Test 55

MTBF Mean Time Between Failures 46, 54, 55, 58, 106, 113, 118

MTTF Mean Time To Failure 46, 58, 99–101, 167

ORT On-going Reliability Test 56

PACVD Plasma-Assisted Chemical Vapor Deposition 14

PC Power Cycling 60–63, 65–67, 70, 73, 75, 102, 123, 126, 127

PCB Printed Circuit Board 21, 54, 73, 74, 115, 165

PDF Probability Density Function 42–44, 47, 48, 50, 94, 99, 102, 125, 164

PEBB Power Electronic Building Block 10, 105–109, 111–117, 121, 122, 125–127, 167, 169

PECVD Plasma-Enhanced Chemical Vapor Deposition 14–16, 163

PFC Power Factor Correction 29

PJ Plasma Jet 19–21, 163

PoC Proof of Concept 51, 52, 54, 57, 113, 115, 116, 121, 124, 125, 167

PoF Physics of Failure 59, 61, 102, 116, 167

PT Plasma Torch 19–21

Pulsed DC Pulsed Direct Current 11, 17, 18, 24, 25, 30–33, 163, 164

PVD Physical Vapor Deposition 9, 11, 14, 16–19, 22, 163

RBD Reliability Block Diagram 54, 113

RF Radio Frequency 11, 16, 18, 25, 27, 33, 34, 164

RIE Reactive Ion Etching 15

ROC Reliability-Oriented Control 106, 114, 126, 167

ROCT Reliability-Oriented Comparative Test 118, 119, 122, 126, 128, 167

RSCC Repetitive Short Circuit Conditions 49, 50

RUL Remaining Useful Lifetime 37–39, 124

SEE Single Event Effects 50, 112

SEPIC Single-Ended Primary Inductor Converter 29

SF Stacking Fault 50

SOA Safe Operating Area 53, 70

SoH State of Health 39, 60, 62, 124

SST Step Stress Test 55

TC Thermal Cycling 60–62, 73

TDDB Time-Dependent Dielectric Breakdown 50, 93

THDi Current Total Harmonic Distortion 28

THDu Voltage Total Harmonic Distortion 28

TPC Temperature and Power Cycling 73, 118, 121

TRUMPF TRUMPF Huettinger Sp. z o.o. 41, 77, 80, 105, 117

TSEP Thermo-Sensitive Electrical Parameter 78, 80

TSV Through-Silicon Via 16, 19

TTM Time To Market 51, 56, 115, 124, 126

UL Useful Lifetime 45–47, 58, 61, 79, 111, 112, 118, 122, 124, 126

UV Ultraviolet 13, 14, 22

VHF Very High Frequency 11, 25, 27, 33

VPE Vapor Phase Epitaxy 14

VSWR Voltage Standing Wave Ratio 33, 35, 123

VUV Vacuum-Ultraviolet 14

WBG Wide-Bandgap 105, 107–109, 112, 113, 115, 167, 169

X-RAY Röntgen Radiation 81, 86, 88, 89, 91, 102, 166

A Material Constant in CIPS2008 model 94

Ag Silver 23

Al Aluminum 24

α Material Constant in CIPS2008 model 94

B Boron 22

β Shape Parameter in the Weibull model 94, 96, 98, 167

β_1 Material Constant in CIPS2008 model 94, 99

β_2 Material Constant in CIPS2008 model 94

β_3 Material Constant in CIPS2008 model 99

C_{GD} Gate-Drain Parasitic Capacitance 115

C_O Correct Operation 82

CrN Chromium Nitride 13

D Diameter of Bonding Wire in the CIPS2008 model 97

E_A Activation Energy 94

η Scale Parameter in the Weibull model 94, 97, 100, 167

f_O Main Output Frequency 26, 163

f_{PULSE} Pulse Frequency 26, 163

$f(x)$ Probability Density Function 42, 94

$F(x)$ Cumulative Density Function 42

γ Location Parameter in the Weibull model 94

GaN Gallium Nitride 16, 107

GaO_X Gallium Oxides 27

h Hours 46

H_2SO_4 Sulfuric Acid 88

I Current per Wire Bond in the CIPS2008 model 97

I_{ACT} Actual Drain-Source Current 82

I_{DS} Drain-Source Current 71, 75–77, 99, 107

$I_{DS_{LKG}}$ Drain-Source Leakage Current 64, 66, 78

$I_{DS_{PEAK}}$ Peak Instantaneous Drain-Source Current 109

$I_{DS_{RMS}}$ Root-Mean-Square Drain-Source Current 109

$I_{GS_{LKG}}$ Gate-Source Leakage Current 64, 66

I_{HIGH} Current Threshold High 81

I_{LOW} Current Threshold Low 81

$I_{NOMINAL}$ Nominal Current 82

$I_{DS_{RPL}}$ Output Current Ripples 75, 76

K Material Constant in CIPS2008 model 94

λ_0 Base Failure Rate 46

λ_{MODULE} Module Failure Rate 113

$\lambda(t)$ Failure Rate 43, 45–47, 56, 58, 113

T_J Junction Temperature 72, 75, 77–80, 165

ΔT_J Amplitude of Junction Temperature Swing 61, 77, 78, 85, 97, 99, 103, 109, 127

$T_{J_{MIN}}$ Minimum Junction Temperature 77

$T_{J_{MAX}}$ Peak Junction Temperature 61, 65, 71, 75, 77, 97, 109

$T_{J_{(n)-(n+1)}}$ Junction Temperature Dispersion Between Neighboring Samples 75–77, 102

$T_{J_{RPL}}$ Junction Temperature Ripples 75, 76

T_{MEAN} Mean Junction Temperature 97

t_{OFF} Pulse Off-time 39, 63, 103, 127

t_{ON} Pulse On-time 39, 63, 97, 103, 127

T_{TOP} Top Surface Temperature 80, 165

V Chip Blocking Voltage in the CIPS2008 model 97

V_{ACT} Actual Drain-Source Voltage 82

V_{CE} On-state Collector-Emitter Voltage Drop 61

V_{DS} Drain-Source Voltage 65, 66, 73, 75, 76, 102, 112, 116, 167

$V_{DS_{MIN}}$ Minimum Drain-Source Voltage 82

$V_{DS_{(n)-(n+1)}}$ Drain-Source Voltage Dispersion Between Neighboring Samples 75–77

$V_{DS_{PEAK}}$ Peak Instantaneous Drain-Source Voltage 109

$V_{DS_{RMS}}$ Root-Mean-Square Drain-Source Voltage 109

V_{DSS} Rated Drain-Source Voltage 71

V_{FB} Flat-band Voltage 65

V_{FWD} Body Diode Forward Voltage Drop 64, 65, 67, 83–85, 88, 165

V_{GS} Gate-Source Voltage 63, 71, 76, 107, 114–116, 167

$V_{GS_{TH}}$ Gate-Source Threshold Voltage 64–66, 78

V_{HIGH} Voltage Threshold High 81

V_{LOW} Voltage Threshold Low 81

$V_{NOMINAL}$ Nominal Voltage 82

V_{OUT} Output Voltage 26, 75, 76, 163

$V_{OUT_{RPL}}$ Output Voltage Ripples 75, 76

V_{REV} Amplitude of Reverse Voltage 26, 163

y Years 46

ZnO Zinc Oxide 23

ZnO_X Zinc Oxides 27

Z_{OUT} Output Impedance 26, 163

$Z_{TH_{JC}}$ Junction-to-Case Thermal Impedance 64–66, 71, 78, 79, 107

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